ADVANCED BIPOLAR LOGIC DATABOOK

NATIONAL SEMICONDUCTOR CORPORATION

ADVANCED BIPOLAR LOGIC DATABOOK

Introduction

This is the Advanced Bipolar Logic Databook from National Semiconductor. The book contains the most up to date information on the Advanced Schottky and Advanced Low Power Schottky families available from National.

Both of these advanced logic families are in their early production phases and will be continually expanded in future National Databook Publications.

Contact your National Semiconductor Representative for more information concerning these next generation logic families or any of the other extensive logic families.

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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A+ Program

A+ Program: A comprehensive program that utilizes National's experience gained from participation in the many Military/Aerospace programs.

A program that not only assures high quality but also increases the reliability of molded integrated circuits.

The A+ program is intended for users who cannot perform incoming inspection of ICs or do not wish to do so, yet need significantly better than usual incoming quality and higher reliability levels for their standard integrated circuits.

Users who specify A+ processed parts will find that the program:

- Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- Reduces the cost of reworking assembed boards.
- Reduces field failures.
- Reduces equipment down time.
- Reduces the need for excess inventories due to yield loss incurred as a result of processing performed at independent testing laboratories.

The A+ Program Saves You Money

It is a widely accepted fact that down-time of equipment is costly not only in lost hours of machine usage but also costly in the reapir and maintenance cycle. One of the added advantages of the A+ program is the burn-in screen, which is one of the most effective screening procedures in the semiconductor industry. Failure rates as a result of the burn-in can be decreased many times. The objective of burn-in is to stress the device much higher that it would be stressed during normal usage.

Reliability vs. Quality

The words "reliability" and "quality" are often used interchangeably, as though they connoted identical facets of a product's merit. But reliability and quality are different, and IC users must understand the essential difference between the two concepts in order to evaluate properly the various vendors' programs for products improvement that are generally available, and National's A+ program in particular.

The concept of quality gives us information about the population and faulty IC devices among good devices, and generally relates to the number of faulty devices that arrive at a user's plant. But looked at in another way, quality can instead relate to the number of faulty ICs that escape detection at the IC vendor's plant.

It is the function of a vendor's Quality Control arm to monitor the degree of success of that vendor in reducing the number of faulty ICs that escape detection. Quality Control does this by testing the outgoing parts on a sampled basis. The Acceptable Quality Level (AQL) in turn determines the stringency of the sampling. As the AQL decreases it becomes more difficult for defective parts to escape detection, thus the quality of the shipped parts increases.

The concept of reliability, on the other hand, refers to how well a part that is initially good will withstand its environment. Reliability is measured by the percentage of parts that fail in a given period of time.

Thus the difference between quality and reliability means the ICs of high quality may, in fact be of low reliability, while those of low quality may be of high reliability.

Improving the Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction: the materials used and the method by which they are assembled.

Reliabilty cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate marginal, short-life parts.

In any test of reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time of failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

National's A+ Program

National has combined the successful B+ program with the Military/Aerospace processing specifications and provides the A+ program as the best practical approach to maximum quality and reliability on molded devices. The following flow chart shows how we do it step by step.

SEM
Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

Epoxy B Processing for All Molded Parts
At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.)

Six Hour, 150°C Bake
This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

High Temperature (100°C) Functional Electrical Test
A high temperature test with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C–30°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient.

Electrical Testing
Every device is tested at 25°C for functional and DC parameters.

Burn-in Test
Devices are stressed at maximum operating conditions to eliminate marginal devices. Test is performed per Mil-Std-883B Method 1015.3.

DC Functional and Parametric Tests
These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Thermal Shock Monitor
Samples from each package type are selected at random each week and submitted to 100 cycles of liquid to liquid thermal shock −65°C to +150°C. In addition, samples are selected every four weeks and subjected to 2000 temperature cycles of 0°C to +25°C.

Tighter-than-normal QC Inspection Plans
Most vendors sample inspect outgoing parts to a 0.3% AQL. When you specify the A+ program, we sample your parts to a 0.035% AQL at room temperature and 0.05% AQL at T_A Max. This eight times tightening (from 0.3 to 0.035% AQL) coupled with three 100% electrical tests, dramatically reduces the number of "escapes" and allows us to guarantee the AQLs listed below.

Ship Parts

Here are the QC sample plans used in our A+ test program:

Test	Temperature	AQL
Electrical Functionality	25°C	0.035%
Parametric, DC	25°C	
Parametric, AC	25°C	0.4%
Electrical Functionality	At each temperature extreme.	0.05%
Parametric, DC		
Mechanical		
Critical	—	0.01%
Major	—	0.28%

B+ Program

B+ Program: a comprehensive program that assures high quality *and* high reliability of molded integrated circuits.

The B+ program improves both the quality *and* the reliability of National's digital, linear, and CMOS Epoxy B integrated circuit products. It is intended for the manufacturing user who cannot perform incoming inspection of ICs, or does not wish to do so, yet needs significantly-better-than-usual incoming quality and reliability levels for standard ICs.

Integrated circuit users who specify B+ processed parts will find that the program:

- Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- Reduces the cost of reworking assembed boards.
- Reduces field failures.
- Reduces equipment down time.

Reliabilty Saves You Money

With the increases population of integrated circuits in modern electronic systems has come an increased concern with IC failures in such systems.

And rightly so, for at least two reasons.

First of all, the effect of component reliability on system reliability can be quite dramatic. For example, suppose that you, as a system manufacturer, were to choose an IC that is 99 percent reliable. You would find that if your system used only 70 such ICs, the overall reliability of the system's IC portion would be only 50 percent. In other words, only one out of two of your systems would operate. The result? A system very costly to produce and probably very difficult to sell.

Secondly, whether the system is large or small you cannot afford to be hounded by the spectre of unnecessary maintenance costs. Not only because labor, repair, and rework costs have risen — and promise to continue to rise — but also because field replacement may be prohibitively expensive. If you ship a system that contains a marginally-performing IC, an IC that later fails in the field, the cost of replacement may be — literally — hundreds of times more than the cost of the failed IC itself.

Improving the Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction: the materials used and the method by which they are assembled.

Now, it's true that reliability cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement, which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate most marginal, short-life parts.

In any test for reliabilty the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time to failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

Quality Improvement

When an IC vendor specifies 100 percent final testing of its parts then, in theory, every shipped part should be a good part. However, in any population of mass-produced items there does exist some small percentage of defective parts.

One of the best ways to reduce the number of such faulty parts is, simply, to retest the parts prior to shipment. Thus, if there is a one percent chance that a bad part will escape detection initially, retesting the parts reduces that probability to only 0.01 percent. (A comparable tightening of the QC group's sampled-test plan ensures the maintenance of the improved quality level.)

National's B+ Program Gets It All Together

We've stated that the B+ program improves both the quality *and* the reliability of National's molded integrated circuits, and pointed out the difference between those two concepts. Now, how do we bring them together? The answer is in the B+ program processing, which is a continuum of stress and double testing. With the exception of the final QC inspection, which is sampled, all steps of the B+ process are performed on 100 percent of the program parts. The following flow chart shows how we do it, step by step.

SEM
Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

Epoxy B Processing for All Molded Parts
At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.)

Six Hour, 150°C Bake
This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

High Temperature (100°C) Functional Electrical Test
A high temperature test such as this with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C —

30°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient. (Even though Epoxy B processing has virtually eliminated thermal intermittents, we perform this test to ensure against even the remote possibility of such a problem. Remember, the emphasis in the B+ program is on the elimination of those marginally-performing devices that would otherwise lower field reliability of the parts.)

DC Functional and Parametric Tests
These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Thermal Shock Monitor
Samples from each package type are selected at random each week and submitted to 100 cycles of liquid to liquid thermal shock −65°C to +150°C. In addition, samples are selected every four weeks and subjected to 2000 temperature cycles of 0°C to +25°C.

Tighter-than-normal QC Inspection Plans
Most vendors sample inspect outgoing parts to a 0.3% AQL. When you specify the B+ program, we sample your parts to a 0.035% AQL at room temperature and 0.05% AQL at T_A Max. This eight times tightening (from 0.3 to 0.035% AQL) coupled with two 100% electrical tests, dramatically reduces the number of "escapes" and allows us to guarantee the AQLs listed below.

Ship Parts

Here are the QC sampling plans used in our B+ test program:

Test	Temperature	AQL
Electrical Functionality	25°C	0.035%
Parametric, DC	25°C	
Parametric, AC	25°C	0.4%
Electrical Functionality	At each temperature extreme.	0.05%
Parametric, DC		
Mechanical		
Critical	—	0.01%
Major	—	0.28%

Advanced Bipolar Logic Data Book
Thermal Ratings for IC's

Maximum Power Dissipation

To insure reliable long term operation of its Integrated Circuits, National Semiconductor has specified maximum junction temperature (Tj) limits. These limits are at 150°C for circuits packaged in a molded dual-in-line package (Epoxy B), and 175°C for all other package types.

Maximum power dissipation (P_D) of an integrated circuit is limited by maximum allowable junction temperature of the silicon die, and the thermal resistance (θ_{J-X}) of the package. *Figure 1* illustrates the relationship between power dissipation and junction temperature.

The line indicating "Maximum Power Rating of Package" is projected from the maximum junction temperature limit (150°C in this example) at a slope corresponding to the package thermal resistance ($1/\theta_{J-X}$). Below this line is the safe operating area of the device. Additional constraints are Maximum Power Dissipation and Maximum Operating Temperature (T_A). These parameters may be determined from device data sheets. For this example, $P_{D(MAX)}$ = 300mW and $T_{A(MAX)}$ = 70°C.

Point "A" in *Figure 1* is an operating point corresponding to T_A = 50°C and P_D = 100mW. Determine device junction temperature by projecting a line from point "A" , parallel to the Maximum Power Rating curve, until it intersects the horizontal axis. Tj is determined from the point of intersection with the horizontal axis. For this example, Tj is 45°C.

Thermal Information

Figure 2 illustrates thermal resistance characteristics for Integrated Circuits packages.

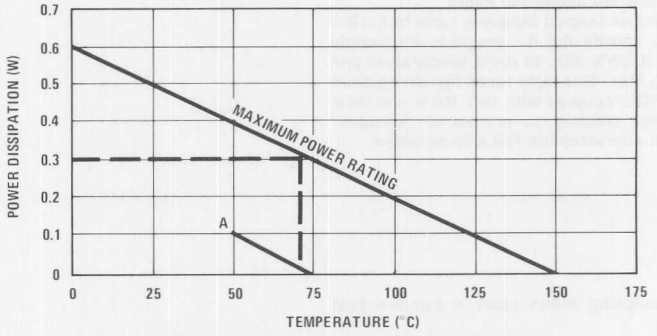


FIGURE 1. Power Dissipation vs Temperature

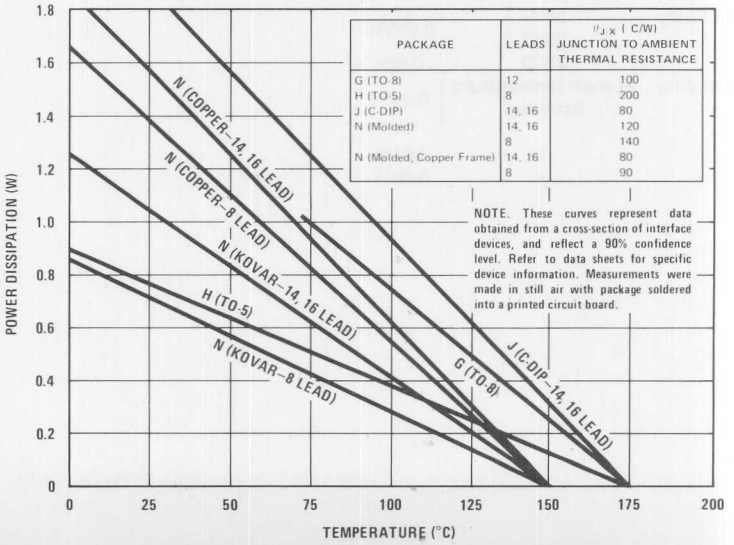
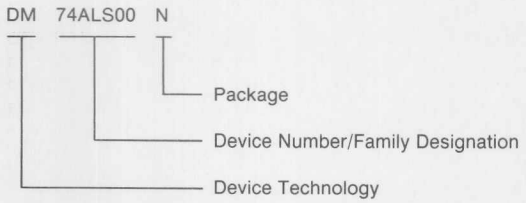


FIGURE 2. Maximum θ_{J-X} Values for IC Packages

Advanced Bipolar Logic Data Book

Ordering Information

Ordering information for National Devices is covered in this catalogue as follows



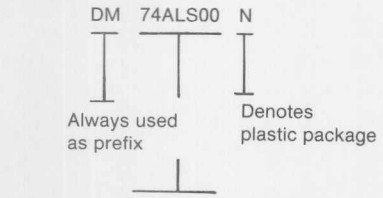
Device Technology

- *DM*—Digital Monolithic

Device Number

- 4 to 8 digit number
- 1st two digits denote temperature selection
  54—denotes full mil range specification −55°C to +125°C
- 74—denotes commercial specification 0°C to 70°C

Example: How to order



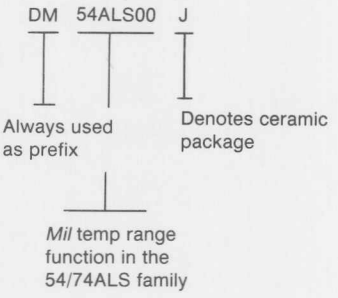
Family Designation

- 54/74ALSXX(X)—Advanced Low Power Schottky
- 54/74ASXX(X)—Advanced Schottky

National Semiconductor manufactures a complete line of industry standard logic products. The industry standard number identifying a particular function is used in marking the product with the only difference being prefixes and suffixes noted above.

When ordering a particular product, please specify the entire number, including the *DM prefix* and appropriate *package* suffix. This will help in processing your order more quickly.

Note: Although the *part* number is generally uniform throughout the industry, competitors vary in terms of denoting package type and temperature selection. Please refer to the industry cross reference guide in the back of this data book for properly cross referencing competitor products.



Advanced Low Power Schottky

The DM54/74ALS family of devices are designed to meet the needs of system designers requiring very low power, higher low level threshold than LS and toggle capability up to 100 MHz. In addition ALS features a 40% reduction in propagation delay times of present LS functions (4ns per gate) while reducing power levels by half (1mw per gate).

In addition to speed improvements, higher threshold, and very low power, the ALS family offers direct TTL/LS replacement functions, ideal for system upgrades and new system designs.

For maximum design flexibility and elimination of special drawings, the ALS family will be introduced with $\pm$ 10% V_{CC} over the military and commercial full temp range as standard product. Furthermore, all switching characteristics are guaranteed over the full temperature and V_{CC} range.

National Semiconductor

ADVANCED LOW POWER SCHOTTKY

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC} (1)	7V
Input Voltage, V_I: All Inputs	7V
I/O Ports	5.5V
Off State (High Level) Voltage Applied to Open-Collector Outputs	7V
High Level Voltage Applied to 3-State Outputs	5.5V
Operating Free-Air Temperature Range:	
SN54ALS	−55°C to 125°C
SN74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Recommended Operating Conditions

Parameter		Standard Output			Buffer Output			Bus Driver Output			Unit
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	54/74ALS	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
High Level Input Voltage, V_{IH}	54/74ALS	2.0			2.0			2.0			V
Low Level Input Voltage, V_{IL}	54/74ALS			0.8			0.8			0.8	V
High Level Output Voltage, I_{OH} (2)	54ALS			−0.4			−1			−12	mA
	74ALS			−0.4			−2.6			−15	mA
High Level Output Current, V_{OH} (3)	54/74ALS			5.5			5.5			5.5	V
Low Level Output Current, I_{OL}	54/74ALS			4			12			12	mA
	74ALS			8			24			24/48	mA
Operating Free-Air Temperature, T_A	54ALS	−55		125	−55		125	−55		125	°C
	74ALS	0		70	0		70	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Parameter		Conditions		Standard Output			Buffer Output			Bus Driver Output			Unit
				Min	Typ(4)	Max	Min	Typ(4)	Max	Min	Typ(4)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5			−1.5			−1.5	V
V_{OH}	High Level Output Voltage (2)	V_{CC} = 4.5V, I_{OH} = MAX					2.4	3.2		2	3.2		V
		V_{CC} = 4.5V, I_{OH} = −3mA								2.4	3.2		V
		I_{OH} = −0.4mA		V_{CC}−2V			V_{CC}−2V			V_{CC}−2V			V
I_{OH}	High Level Output Current (3)	V_{CC} = 4.5V V_{OH} = 5.5V				0.1			0.1			0.1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = MAX	74ALS		0.35	0.5		0.35	0.5		0.35	0.5	V
			54/74ALS		0.25	0.4		0.25	0.4		0.25	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V V_I = 7V				0.1			0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_I = 2.7V				20			20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V			−0.02	−0.2		−0.05	−0.2		−0.05	−0.2	mA
I_O	Output Current (5)	V_{CC} = 5.5V V_O = 2.25V		−30		−110	−30		−110	−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied (6)	V_{CC} = 5.5V V_O = 2.7V							20			20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied (6)	V_{CC} = 5.5V V_O = 0.4V	I/O Ports						−0.2			−0.2	mA
			Non-I/O						−20			−20	μA
I_{CC}	Supply Current (7)	V_{CC} = 5.5V											mA

NOTE 1: Voltage values are with respect to network ground terminal.
NOTE 2: Does not apply to open-collector outputs.
NOTE 3: Applies only to open-collector outputs.
NOTE 4: All typical numbers are at V_{CC} = 5V, T_A = 25°C.
NOTE 5: The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.
NOTE 6: Applies only to TRI-STATE outputs.
NOTE 7: Refer to individual data sheet for I_{CC} limits.

National Semiconductor

Preliminary

DM54ALS00/DM74ALS00 Quad 2-Input NAND Gates

Features

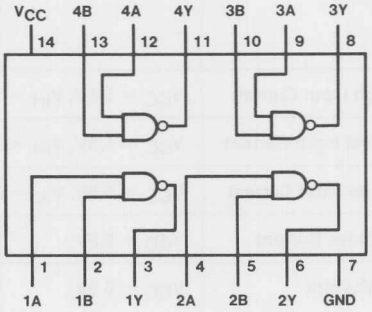
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{AB}$



54ALS00 (J) 74ALS00 (J,N)

1

Recommended Operating Conditions

Parameter	DM54ALS00			DM74ALS00			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.43	0.85	mA
			Outputs Low		1.62	3.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS00			DM74ALS00			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	2	4	10	2	4	9	ns
T_{PHL}, Propagation delay time. High to low level output		2	4	10	2	4	9	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS01/DM74ALS01 Quad 2-Input NAND Gates with Open Collector Outputs

Features

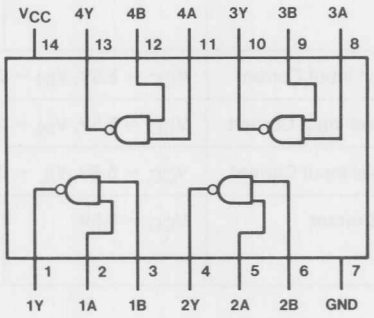
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Off State (High Level)	7V
Output Voltage	
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{AB}$



54ALS01 (J) 74ALS01 (J,N)

1

Recommended Operating Conditions

Parameter	DM54ALS01			DM74ALS01			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.43	0.85	mA
			Outputs Low		1.62	3.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS01			DM74ALS01			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 2K Ω, C_L = 50 pF.	23	27	59	23	27	54	ns
T_{PHL}, Propagation delay time. High to low level output		4	7	25	4	7	20	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-4.

National Semiconductor

Preliminary

DM54ALS02/DM74ALS02 Quad 2-Input NOR Gates

Features

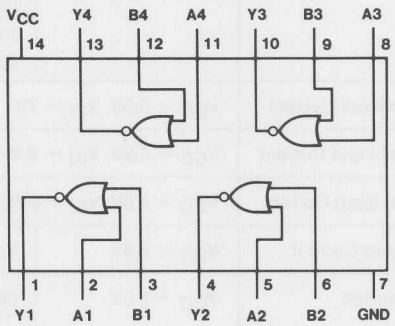
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$$Y = \overline{A + B}$$



54ALS02 (J) 74ALS02 (J,N)

1

Recommended Operating Conditions

Parameter	DM54ALS02			DM74ALS02			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.85	2.2	mA
			Outputs Low		2.16	4.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS02			DM74ALS02			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	2	5	11	2	5	10	ns
T_{PHL}, Propagation delay time. High to low level output		2	5	10	2	5	9	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS03/DM74ALS03 Quad 2-Input NAND Gates with Open Collector Outputs

Features

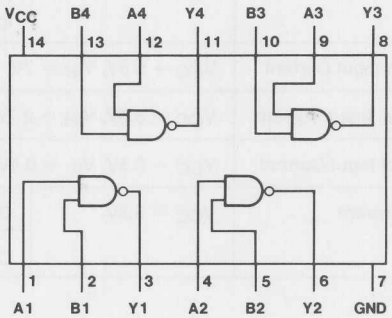
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Off State (High Level)	
Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{AB}$



54ALS03 (J) 74ALS03 (J,N)

1

Recommended Operating Conditions

Parameter	DM54ALS03			DM74ALS03			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.43	0.85	mA
			Outputs Low		1.62	3.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS03			DM74ALS03			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V, R_L = 2K Ω, C_L = 50 pF.	23	27	59	23	27	54	ns
T_{PHL}, Propagation delay time. High to low level output		4	7	25	4	7	20	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-4.

National Semiconductor

Preliminary

DM54ALS04/DM74ALS04 Hex Inverters

Features

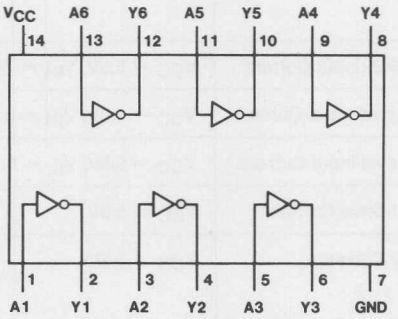
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{A}$



54ALS04 (J) 74ALS04 (J,N)

1

Recommended Operating Conditions

Parameter	DM54ALS04			DM74ALS04			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.65	1.1	mA
			Outputs Low		2.4	3.8	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS04			DM74ALS04			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	2	4	10	2	4	9	ns
T_{PHL}, Propagation delay time. High to low level output		2	4	9	2	4	8	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS05/DM74ALS05 Hex Inverters with Open Collector Outputs

Features

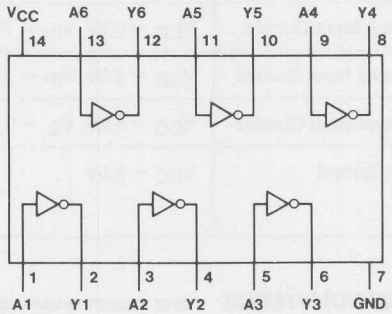
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Off State (High Level)	7V
Output Voltage	
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{A}$



54ALS05 (J) 74ALS05 (J,N)

1

Recommended Operating Conditions

Parameter	DM54ALS05			DM74ALS05			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.65	1.1	mA
			Outputs Low		2.4	3.8	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS05			DM74ALS05			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V, R_L = 2K Ω, C_L = 50 pF.	23	27	59	23	27	54	ns
T_{PHL}, Propagation delay time. High to low level output		4	7	24	4	7	19	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-4.

National Semiconductor

Preliminary

DM54ALS08/DM74ALS08 Quad 2-Input AND Gates

Features

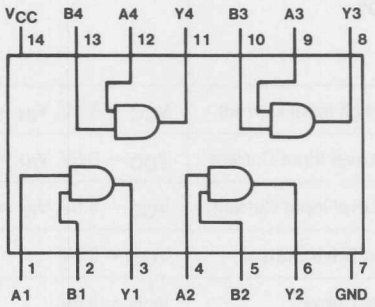
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

Y = AB



54ALS08 (J) 74ALS08 (J,N)

1

Recommended Operating Conditions

Parameter	DM54ALS08			DM74ALS08			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1.3	2.4	mA
			Outputs Low		2.2	4.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS08			DM74ALS08			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	3	5	13	3	5	12	ns
T_{PHL}, Propagation delay time. High to low level output		3	5	11	3	5	10	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS09/DM74ALS09 Quad 2-Input AND Gates with Open Collector Outputs

Features

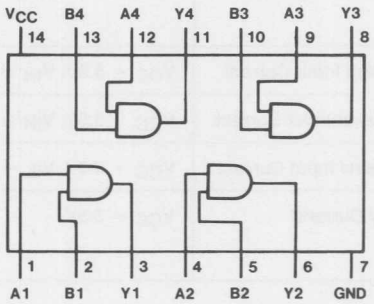
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Off State (High Level)	
Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

Y = AB



54ALS09 (J) 74ALS09 (J,N)

1

Recommended Operating Conditions

Parameter	DM54ALS09			DM74ALS09			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1.3	2.4	mA
			Outputs Low		2.2	4.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS09			DM74ALS09			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 2K Ω, C_L = 50 pF.	23	27	59	23	27	54	ns
T_{PHL}, Propagation delay time. High to low level output		4	7	14	4	7	13	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-4.

National Semiconductor

Preliminary

DM54ALS10/DM74ALS10 Triple 3-Input NAND Gates

Features

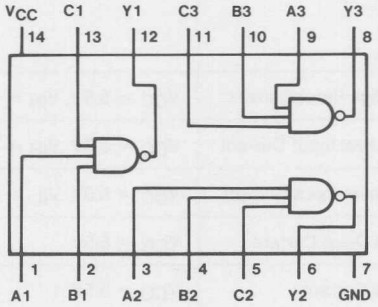
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{ABC}$



54ALS10 (J) 74ALS10 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS10			DM74ALS10			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.32	0.6	mA
			Outputs Low		1.2	2.2	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS10			DM74ALS10			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	2	4	10	2	4	9	ns
T_{PHL}, Propagation delay time. High to low level output		2	6	14	2	6	12	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS11/DM74ALS11 Triple 3-Input AND Gates

Features

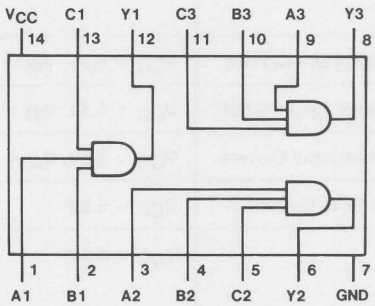
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

Y = ABC



54ALS11 (J) 74ALS11 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS11			DM74ALS11			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}		V_{CC} = 5.5V	Outputs High		1.0	1.8	mA
			Outputs Low		1.6	3.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS11			DM74ALS11			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	3	5	17	3	5	15	ns
T_{PHL}, Propagation delay time. High to low level output		3	6	11	3	6	10	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS12/DM74ALS12 Triple 3-Input NAND Gates with Open Collector Outputs

Features

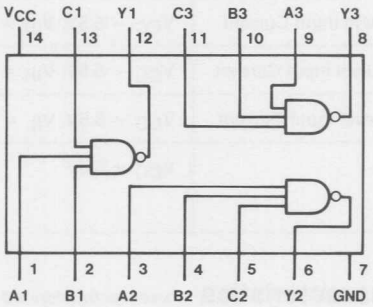
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Off State (High Level)	
Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{ABC}$



54ALS12 (J) 74ALS12 (J,N)

1

Recommended Operating Conditions

Parameter	DM54ALS12			DM74ALS12			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_{CC}		V_{CC} = 5.5V	Outputs High		0.32	0.6	mA
			Outputs Low		1.2	2.2	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS12			DM74ALS12			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	23	27	54	23	27	59	ns
T_{PHL}, Propagation delay time. High to low level output		5	8	29	5	8	23	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-4.

National Semiconductor

Preliminary

DM54ALS15/DM74ALS15 Triple 3-Input AND Gates with Open Collector Outputs

Features

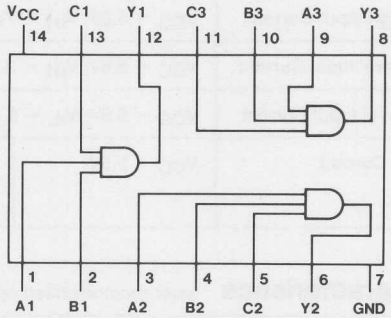
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Off State (High Level) Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

Y = ABC



54ALS15 (J) 74ALS15 (J,N)

1

Recommended Operating Conditions

Parameter	DM54ALS15			DM74ALS15			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1.0	1.8	mA
			Outputs Low		1.66	3.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS15			DM74ALS15			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 2K Ω, C_L = 50 pF.	23	27	59	23	27	54	ns
T_{PHL}, Propagation delay time. High to low level output		4	7	14	4	7	13	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-4.

National Semiconductor

Preliminary

DM54ALS20/DM74ALS20 Dual 4-Input NAND Gates

Features

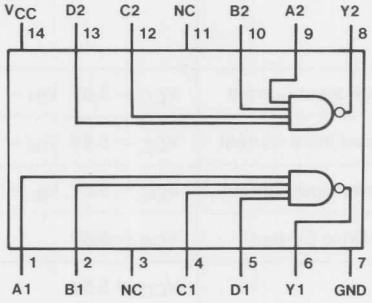
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{ABCD}$



54ALS20 (J) 74ALS20 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS20			DM74ALS20			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}		V_{CC} = 5.5V	Outputs High		0.22	0.4	mA
			Outputs Low		0.81	1.5	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS20			DM74ALS20			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	2	4	10	2	4	9	ns
T_{PHL}, Propagation delay time. High to low level output		5	9	17	5	9	15	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS21/DM74ALS21 Dual 4-Input AND Gates

Features

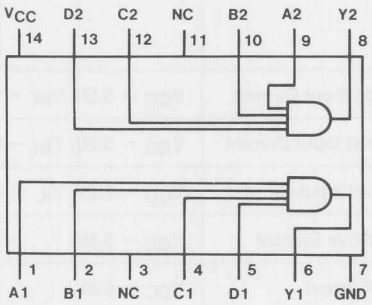
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

Y = ABCD



54ALS21 (J) 74ALS21 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS21			DM74ALS21			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.67	1.2	mA
			Outputs Low		1.10	2.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS21			DM74ALS21			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	5	8	20	5	8	18	ns
T_{PHL}, Propagation delay time. High to low level output		3	6	11	3	6	10	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS22/DM74ALS22 Dual 4-Input NAND Gates with Open Collector Outputs

Features

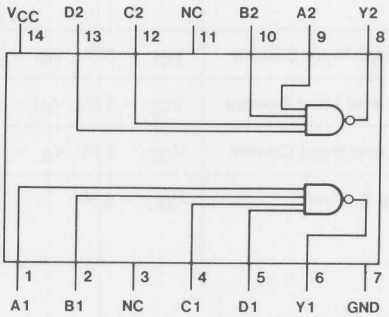
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Off State (High Level)	
Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{ABCD}$



54ALS22 (J) 74ALS22 (J,N)

1

Recommended Operating Conditions

Parameter	DM54ALS22			DM74ALS22			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.22	0.4	mA
			Outputs Low		0.80	1.5	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS22			DM74ALS22			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V, R_L = 2K Ω, C_L = 50 pF.	23	27	59	23	27	54	ns
T_{PHL}, Propagation delay time. High to low level output		8	11	32	8	11	26	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-4.

National Semiconductor

Preliminary

DM54ALS27/DM74ALS27 Triple 3-Input NOR Gates

Features

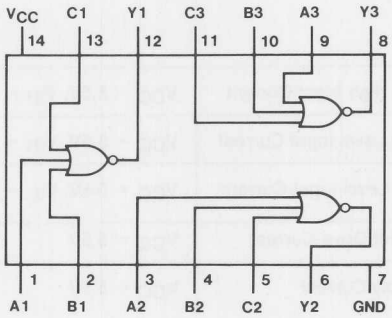
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$$Y = \overline{A+B+C}$$



54ALS27 (J) 74ALS27 (J,N)

1

Recommended Operating Conditions

Parameter	DM54ALS27			DM74ALS27			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.97	1.8	mA
			Outputs Low		2.0	4.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS27			DM74ALS27			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	2	8	15	2	8	13	ns
T_{PHL}, Propagation delay time. High to low level output		2	3	10	2	3	9	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS28/DM74ALS28 Quadruple 2-Input NOR Buffers

Features

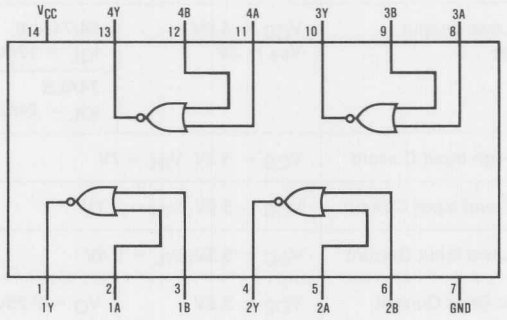
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS28.
- Improved Line Receiving Characteristics.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS28	−55°C to 125°C
DM74ALS28	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{A+B}$



54ALS28 (J) **74ALS28 (J,N)**

Recommended Operating Conditions

Parameter	DM54ALS28			DM74ALS28			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Nom	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			1.7	2.8	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			4.8	8.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS28			DM74ALS28			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	2		10	2		8	ns
T_{PHL}, Propagation delay time. High to low level output		3		10	3		8	ns

NOTE 1: See notes pg. 1-iii, Figures pg. 3-1.

Preliminary

National Semiconductor

DM54ALS30/DM74ALS30 8 Input NAND Gate

Features

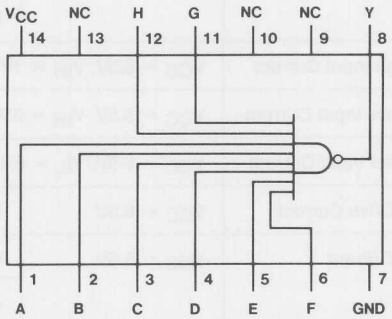
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$$Y = \overline{ABCDEFGH}$$



54ALS30 (J) 74ALS30 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS30			DM74ALS30			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.4	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.22	0.36	mA
			Outputs Low		0.54	0.90	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS30			DM74ALS30			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	2	4	10	2	4	9	ns
T_{PHL}, Propagation delay time. High to low level output		5	9	17	5	9	15	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS32/DM74ALS32 Quad 2-Input OR Gates

Features

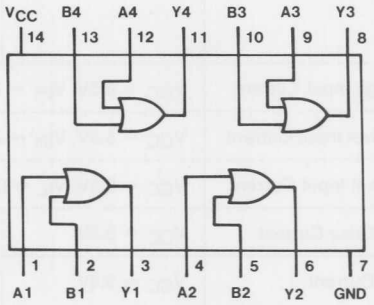
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = A + B$



54ALS32 (J) 74ALS32 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS32			DM74ALS32			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1.9	4.0	mA
			Outputs Low		2.6	4.9	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS32			DM74ALS32			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	3	6	13	3	6	12	ns
T_{PHL}, Propagation delay time. High to low level output		2	5	12	2	5	11	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS33/DM74ALS33 Quadruple 2-Input NOR Buffers with Open-Collector Outputs

Features

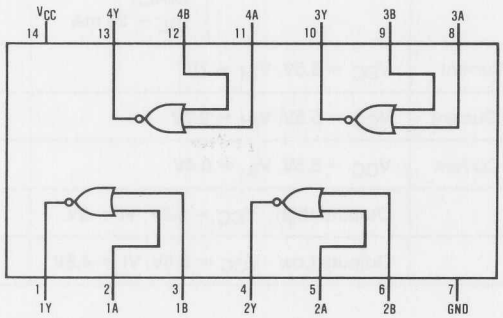
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced, Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS33.
- Improved Line Receiving Characteristics.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Off State (High Level) Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS33	−55°C to 125°C
DM74ALS33	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{A+B}$



54ALS33 (J) **74ALS33 (J,N)**

1

Recommended Operating Conditions

Parameter	DM54ALS33			DM74ALS33			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			1.7	2.8	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			4.8	8.	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS33			DM74ALS33			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5V to 5.5V R_L = 667 Ω C_L = 50 pF	10		40	10		30	ns
T_{PHL}, Propagation delay time. High to low level output		7		18	7		15	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-4.

National Semiconductor

Preliminary

DM54ALS37/DM74ALS37 Quadruple 2-Input NAND Buffers

Features

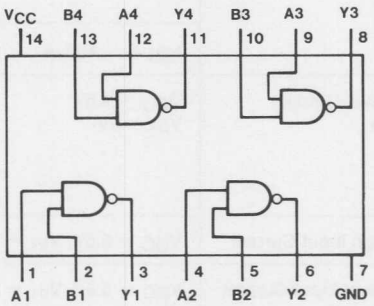
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced, Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS37.
- Improved Line Receiving Characteristics.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS37	−55°C to 125°C
DM74ALS37	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{AB}$



54ALS37 (J) 74ALS37 (J,N)

1

Recommended Operating Conditions

Parameter	DM54ALS37			DM74ALS37			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			0.86	1.6	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			4.0	6.4	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS37			DM74ALS37			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω C_L = 50 pF	2		10	2		8	ns
T_{PHL}, Propagation delay time. High to low level output		3		10	3		8	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS38/DM74ALS38 Quadruple 2-Input NAND Buffers with Open-Collector Outputs

Features

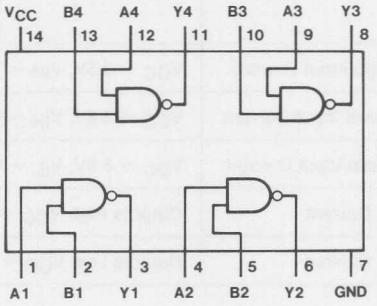
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS38.
- Improved Line Receiving Characteristics.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Off State (High Level) Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS38	−55°C to 125°C
DM74ALS38	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{AB}$



54ALS38 (J) 74ALS38 (J,N)

1

Recommended Operating Conditions

Parameter	DM54ALS38			DM74ALS38			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	VCC = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			0.86	1.6	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			4.0	6.4	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS38			DM74ALS38			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 667 Ω, C_L = 50 pF	10		40	10		30	ns
T_{PHL}, Propagation delay time. High to low level output		7		18	7		15	ns

NOTE 1: See notes pg. 1-iii, Figures pg. 3-4.

National Semiconductor

Preliminary

DM54ALS40/DM74ALS40 Dual 4-Input NAND Buffers

Features

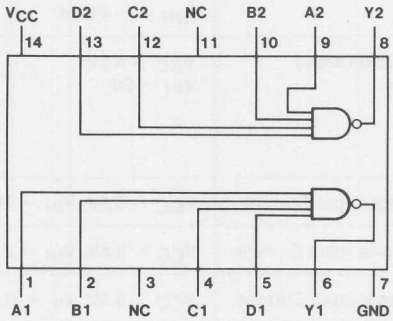
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS40.
- Improved Line Receiving Characteristics.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS40	−55°C to 125°C
DM74ALS40	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{ABCD}$



54ALS40 (J) 74ALS40 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS40			DM74ALS40			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = -2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			0.43	0.8	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			2.0	3.2	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS40			DM74ALS40			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	2		10	2		8	ns
T_{PHL}, Propagation delay time. High to low level output		3		10	3		8	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

Preliminary

National Semiconductor

DM54ALS74/DM74ALS74 Dual D Positive-Edge-Triggered Flip-Flops with Preset and Clear

General Description

The DM54ALS74 is a dual edge-triggered flip-flops. Each flip-flop has individual D, clock, clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D input signal has no effect.

Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

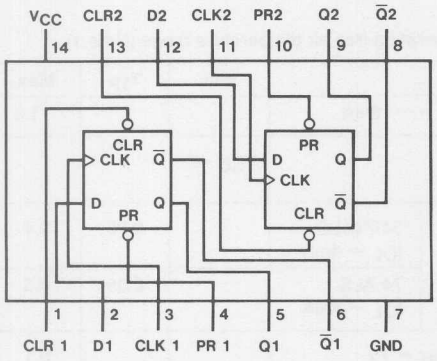
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-For-Pin Compatible with Schottky and LS TTL Counterpart.
- Improved AC Performance Over LS74 at Approximately Half the Power.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS74 (J) 74ALS74 (J,N)

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Q_0 = Previous Condition of Q
* = This condition is nonstable; it will not persist when preset and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

1

Recommended Operating Conditions

Parameter		DM54ALS74			DM74ALS74			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−0.4			−0.4	mA
Low Level Output Current, I_{OL}				4			8	mA
Clock frequency, f_{CLOCK}		0		30	0		34	MHz
Width of Clock Pulse, T_W	High	14			12			ns
	Low	19			17			ns
Pulse Width T_W, Preset & Clear	Low	15			15			ns
Data Setup Time, T_{SU}	Data	15↑			15↑			ns
	PRE or CLR Inactive	10↑			10↑			ns
Data Hold Time, T_H		0↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

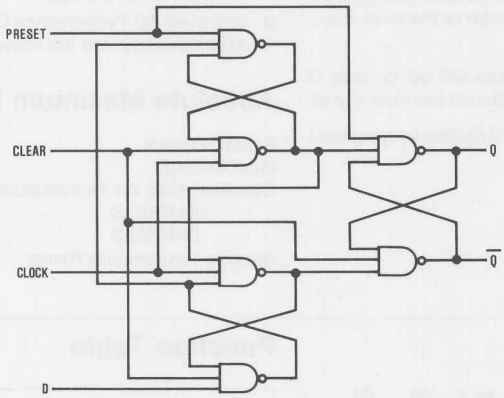
	Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage		I_{OH} = −400μA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage		V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 4mA		0.25	0.4	V
				74 ALS I_{OL} = 8mA		0.35	0.5	V
I_I	Max High Input Current		V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	Clock, D	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
		Preset, Clear					40	μA
I_{IL}	Low Level Input Current	Clock, D	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
		Preset, Clear					−0.4	mA
I_O	Output Drive Current		V_{CC} = 5.5V V_O = 2.25V		−30		−110	mA
I_{CC}	Supply Current		V_{CC} = 5.5V			2.4	4	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS74			DM74ALS74			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	30			34			MHz
T_{PLH}	Preset or clear	Q		2	5	11	2	5	10	ns
T_{PHL}				4	8	15	4	8	13	ns
T_{PLH}	Clock	Q		4	7	16	4	7	14	ns
T_{PHL}				5	10	20	5	10	17	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-3.

Logic Diagram



National Semiconductor

Preliminary

DM54ALS109/DM74ALS109 Dual J-$\overline{K}$ Positive-Edge-Triggered Flip-Flops with Preset and Clear

General Description

The DM54ALS109 is a dual edge-triggered flip flops. Each flip flop has individual J, $\overline{K}$, clock, clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input J or $\overline{K}$ is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the J, $\overline{K}$ input signal has no effect.

Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

The J$\overline{K}$ design allows operation as a D flip flop by tying the J and $\overline{K}$ inputs together.

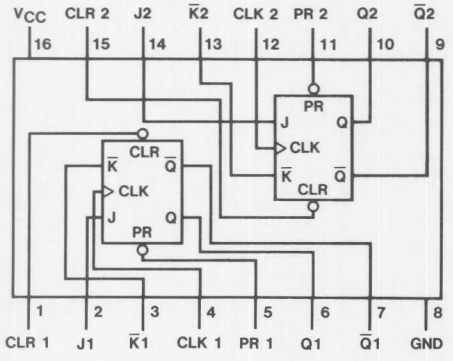
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and LS TTL Counterpart.
- Improved AC Performance Over LS109 at Approximately Half the Power.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS109 (J) 74ALS109 (J,N)

Function Table

Inputs					Outputs	
PR	CLR	CK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition, Q_0 = Previous Condition of Q

* This condition is nonstable; it will not persist when present and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Recommended Operating Conditions

Parameter		DM54ALS109			DM74ALS109			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−0.4			−0.4	mA
Low Level Output Current, I_{OL}				4			8	mA
Clock Frequency, fCLOCK		0		30	0		34	MHz
Pulse Width T_W	Clock High	14			12			ns
	Clock Low	19			17			ns
Pulse Width T_W, Preset & Clear		15			15			ns
Data Setup Time, T_{SU}	J or $\overline{K}$	15↑			15↑			ns
	PRE or CLR inactive	10↑			10↑			
Data Hold Time, T_H		0↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

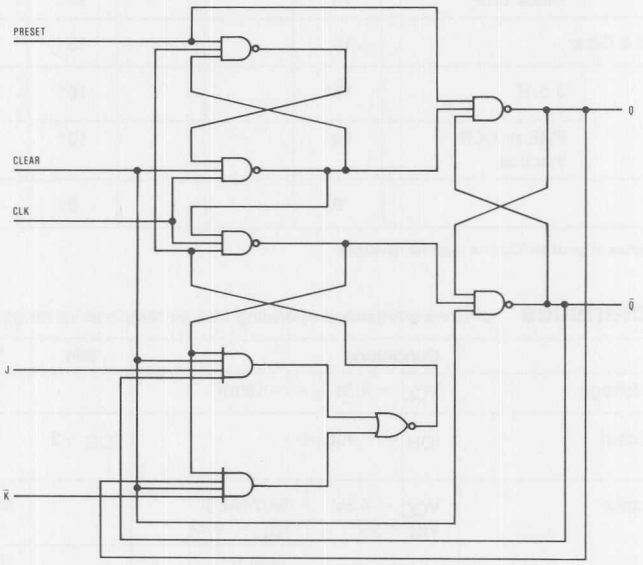
	Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage		I_{OH} = −400μA		V_{CC} −2			V
V_{OL}	Low Level Output Voltage		V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 4mA		0.25	0.4	V
				74ALS I_{OL} = 8mA		0.35	0.5	V
I_I	Max High Input Current		V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	Clock, J, $\overline{K}$	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
		Preset, Clear					40	
I_{IL}	Low Level Input Current	Clock, J, $\overline{K}$	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
		Preset, Clear					−0.4	
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V		−30		−110	mA
I_{CC}	Supply Current		V_{CC} = 5.5V			2.4	4	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS109			DM74ALS109			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	30	50		34	50		MHz
T_{PLH}	Preset or clear	Q		2	5	11	2	5	10	ns
T_{PHL}				4	8	15	4	8	13	ns
T_{PLH}	Clock	Q		4	7	16	4	7	14	ns
T_{PHL}				5	10	20	5	10	17	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-3.

Logic Diagram



National Semiconductor

Preliminary

DM54ALS131/DM74ALS131
3-Line to 8-Line Decoder/Demultiplexer with Address Register

General Description

The ALS131 is a three-line to eight-line decoder/demultiplexer with registers on the three address inputs. When the clock transitions from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. The output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or clock inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The ALS131 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

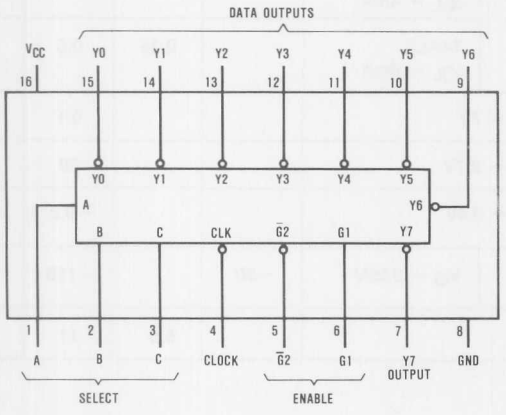
Features

- Combines Decoder and 3-Bit Address Register.
- Incorporates 3 Enable Inputs to Simplify Cascading.
- Low Power Dissipation . . . 28mW Typ
- Switching Specification Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS131	−55°C to 125°C
DM74ALS131	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS131 (J) 74ALS131 (J,N)

Function Table

Inputs						Outputs							
			Select										
CLK	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
↑	H	L	L	L	L	L	H	H	H	H	H	H	H
↑	H	L	L	L	H	H	L	H	H	H	H	H	H
↑	H	L	H	H	L	H	H	L	H	H	H	H	H
↑	H	L	L	H	H	H	H	H	L	H	H	H	H
↑	H	L	H	L	L	H	H	H	H	L	H	H	H
↑	H	L	H	L	H	H	H	H	H	H	L	H	H
↑	H	L	H	L	H	H	H	H	H	H	L	H	H
↑	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	X	X	X	Output corresponding to stored address, L; all others, H.							

H = High Level, L = Low Level, X = Don't Care
↑ = Transition from Low to High Level

Recommended Operating Conditions

Parameter		DM54ALS131			DM74ALS131			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−0.4			−0.4	mA
Low Level Output Current, I_{OL}				4			8	mA
Clock Frequency, F_{CLOCK}		0		40	0		50	MHz
Width of Clock Pulse, T_W		15			10			ns
Setup Time, T_{SU}	A, B, C	15↑			10↑			ns
Hold Time, T_H	A, B, C	0↑			0↑			ns

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4mA		0.25	0.4	V
			74ALS I_{OL} = 8mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			5.5	11	mA

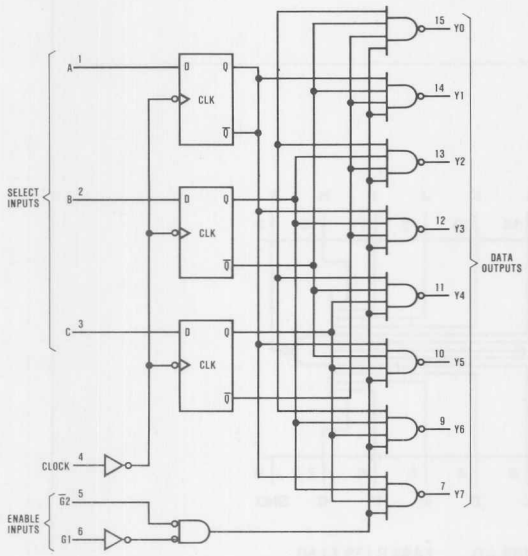
Switching Characteristics

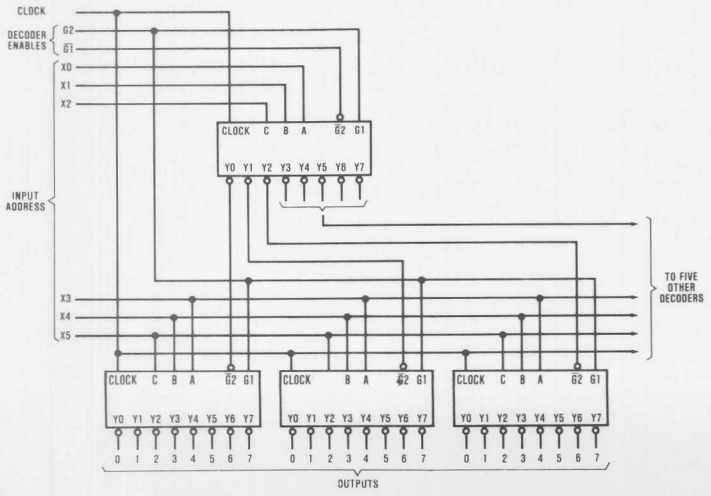
over recommended operating free air temperature range (Note 1)

Parameter	From (Input)	Conditions	DM54ALS131			DM74ALS131			Unit
			Min	Typ	Max	Min	Typ	Max	
T_{PLH}	$\overline{G2}$	V_{CC} = 4.5 to 5.5V R_L = 500 Ω C_L = 50 pF	5	7	18	5	7	15	ns
T_{PHL}			5	7.5	18	5	7.5	15	
T_{PLH}	G1		7	10	24	7	10	20	
T_{PHL}			6	10	20	6	10	17	
T_{PLH}	Clock		8	10	26	8	10	23	
T_{PHL}			7	10	24	7	10	20	ns

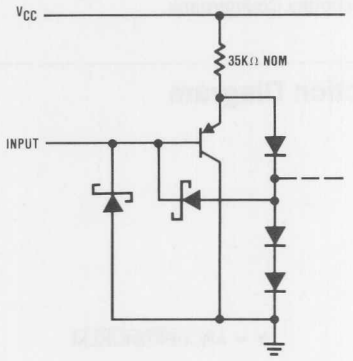
NOTE 1: See notes pg. 1-iii, figures pg. 3-3.

Logic Diagrams





Schematic Diagram



National Semiconductor

Preliminary

DM54ALS133/DM74ALS133 13-Input NAND Gate

Features

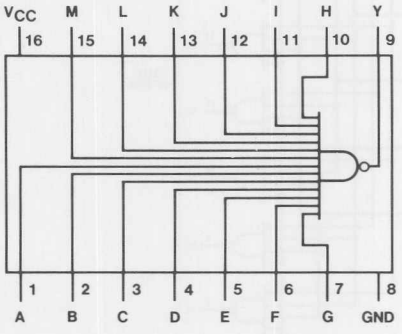
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$$Y = \overline{ABCDEFGHIJKLM}$$



54ALS133 (J) 74ALS133 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS133			DM74ALS133			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4mA		0.25	0.4	V
			74 ALS I_{OL} = 8mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.4	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.24	0.34	mA
			Outputs Low		0.56	0.80	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS133			DM74ALS133			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	2	4	10	2	4	9	ns
T_{PHL}, Propagation delay time. High to low Level Output		5	10	25	5	10	22	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS137/DM74ALS137 3-Line to 8-Line Decoder/Demultiplexer with Address Latches

General Description

The ALS137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the ALS137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The ALS137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

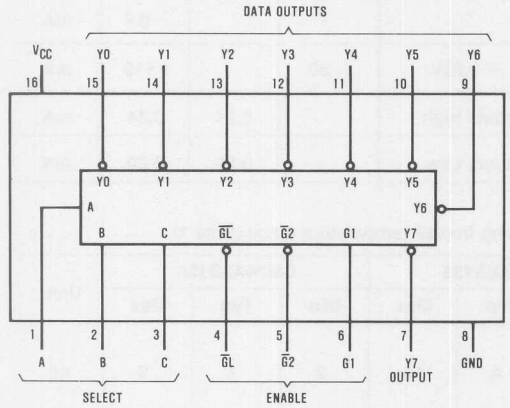
Features

- Combines Decoder and 3-Bit Address Latch.
- Incorporates 3 Enable Inputs to Simplify Cascading.
- Low Power Dissipation . . . 28 mW Typ.
- Switching Specifications Guaranteed over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS137	−55°C to 125°C
DM74ALS137	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS137 (J) 74ALS137 (J,N)

Function Table

Inputs						Outputs							
Enable			Select										
GL	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

L = Low State, H = High State, X = Don't Care

Recommended Operating Conditions

Parameter		DM54ALS137			DM74ALS137			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−0.4			−0.4	mA
Low Level Output Current, I_{OL}				4			8	mA
Width of Enabling Pulse, T_W	$\overline{GL}$	15			10			ns
Setup Time, T_{SU}	A, B, C	15↑			10↑			ns
Hold Time, T_H	A, B, C	5↑			5↑			ns

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

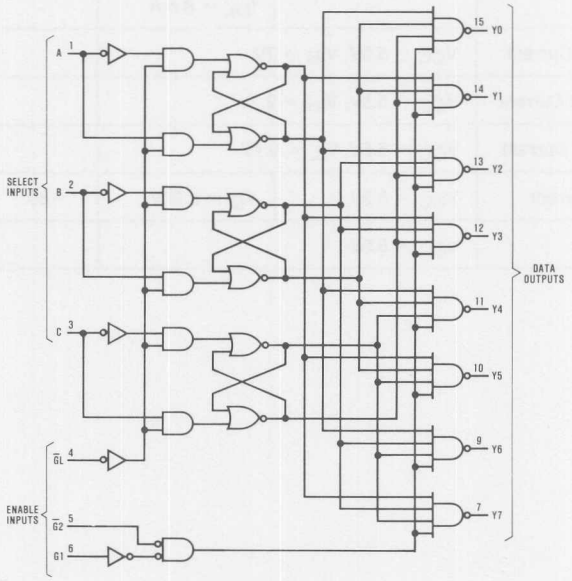
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = 0.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			5	10	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

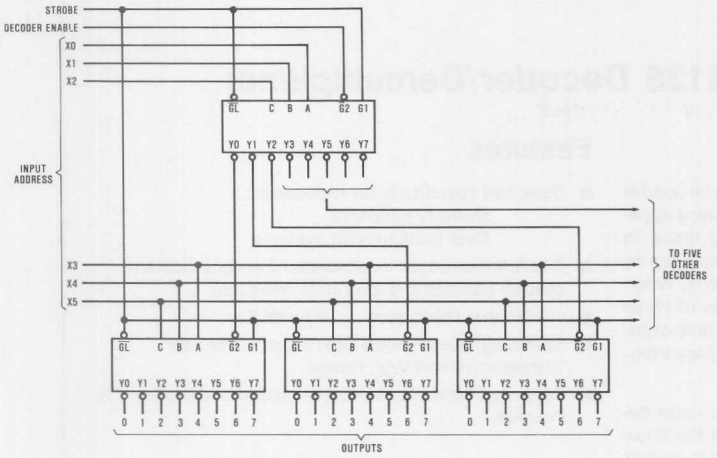
Parameter	From (Input)	Conditions	DM54ALS137			DM74ALS137			Unit
			Min	Typ	Max	Min	Typ	Max	
T_{PLH}	A, B, C 3 Levels of Delay	V_{CC} = 4.5 to 5.5V R_L = 500 Ω C_L = 50 pF.	3	9	20	3	9	16	ns
T_{PHL}			4	10	25	4	10	20	
T_{PLH}	A, B, C 4 Levels of Delay		4	12	25	4	12	20	
T_{PHL}			5	13	25	5	13	20	
T_{PLH}	G2		4	7.5	15	4	7.5	12	
T_{PHL}			5	7.5	18	5	7.5	15	
T_{PLH}	G1		5	10	21	5	10	17	
T_{PHL}			5	10	19	5	10	15	
T_{PLH}	$\overline{GL}$		7	13	25	7	13	20	
T_{PHL}			7	13	25	7	13	20	ns

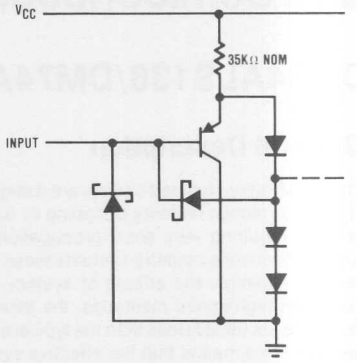
NOTE 1: See notes pg. 1-iii, figures pg. 3-3.

Logic Diagrams



Logic Diagrams





National Semiconductor

Preliminary

DM54ALS138/DM74ALS138 Decoder/Demultiplexer

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The ALS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

This decoder/demultiplexer features fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

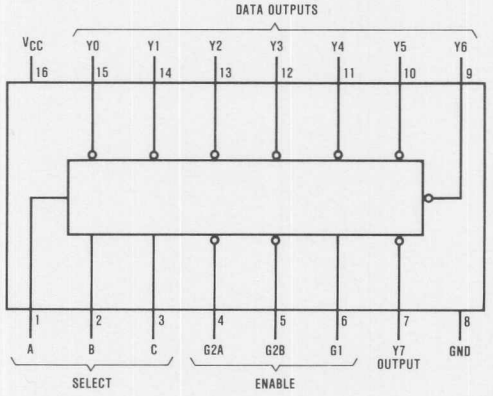
Features

- Designed specifically for high-speed:
  - Memory decoders
  - Data transmission systems
- 3-to-8-line decoder incorporates 3 enable inputs to simplify cascading and/or data reception.
- Low Power Dissipation . . . 23 mW Typ.
- Switching Specification Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS138 (J) **74ALS138 (J,N)**

Recommended Operating Conditions

Parameter	DM54ALS138			DM74ALS138			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−0.4			−0.4	mA
Low Level Output Current, I_{OL}			4			8	mA

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

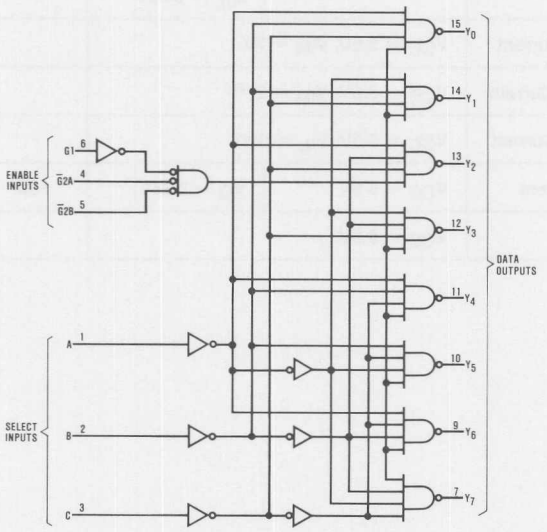
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = 0.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			5	10	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From (Input)	Conditions	DM54ALS138			DM74ALS138			Unit
			Min	Typ	Max	Min	Typ	Max	
T_{PLH}	A, B, C 4 Levels of Delay	V_{CC} = 4.5 to 5.5V R_L = 500 Ω C_L = 50 pF.	7	7.5	25	7	7.5	20	ns
T_{PHL}			6	8	22	6	8	18	
T_{PLH}	A, B, C 3 Levels of Delay		6	8.5	21	6	8.5	18	
T_{PHL}			6	7.5	21	6	8.5	18	
T_{PLH}	Enable $\overline{G2}$		4	6	15	4	6	13	
T_{PHL}			5	8	19	5	8	15	
T_{PLH}	Enable G1		5	8.5	20	5	8.5	17	
T_{PHL}			6	8	20	6	8	17	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

Logic Diagram



National Semiconductor

Preliminary

DM54ALS151/DM74ALS151 8-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-eight data sources as a result of a unique three-bit binary code at the Select inputs. Two complementary outputs provide both inverting and non-inverting buffer operation. A Strobe input is provided which, when at the high level, disables all data inputs and forces the Y output to the low state and the W output to the high state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

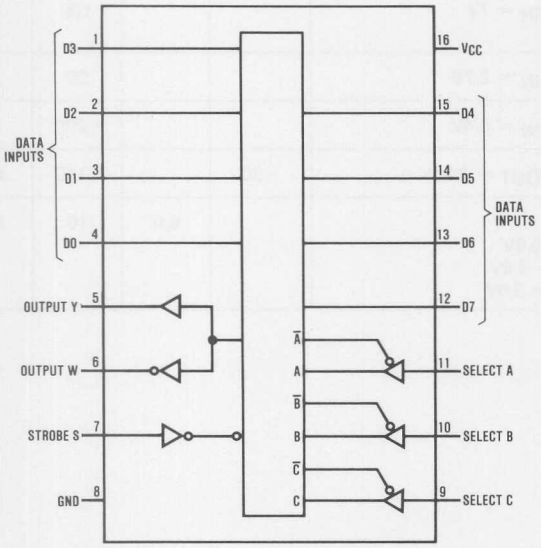
Features

- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL process.
- Switching Performance is Guaranteed Over Full Temperature and V_{CC} Supply Range.
- Pin and Functional Compatible with LS Family Counterpart.
- Improved Output Transient Handling Capability.

Absolute Maximum Ratings

Supply Voltage	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54ALS151	−55°C to 125°C
DM74ALS151	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Connection Diagram



54ALS151 (J) 74ALS151 (J,N)

Function Table

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level L = Low Level X = Don't Care
D0 thru D7 = the level of the respective D input

1

Recommended Operating Conditions

Parameter	DM54ALS151			DM74ALS151			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5		5.5	4.5		5.5	V
High Level Input Voltage, V_{IH}	2.0			2.0			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

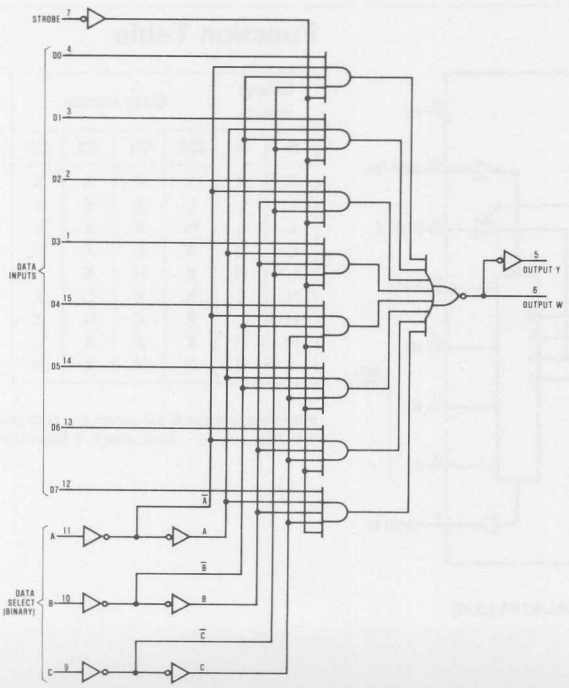
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		IOH = −400μA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54ALS/74ALS I_{OL} = 12mA		.25	.40	V
			74ALS I_{OL} = 24mA		.35	.50	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−200	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V Date Inputs = 3.0V Select Inputs = 3.0V Strobe Inputs = 3.0V			6.0	10	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS151			DM74ALS151			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V C_L = 50 pF R_L = 500 Ω		7.5			7.5		ns
t_{PHL}, High to low Level Output					9.0			9.0		ns
t_{PLH}, Low to high Level Output		W			9.0			9.0		ns
t_{PHL}, High to low Level Output					9.5			9.5		ns
t_{PLH}, Low to high Level Output	Data	Y			4.0			4.0		ns
t_{PHL}, High to low Level Output					6.0			6.0		ns
t_{PLH}, Low to high Level Output		W			6.0			6.0		ns
t_{PHL}, High to low Level Output					6.0			6.0		ns
t_{PLH}, Low to high Level Output	Strobe	Y			4.0			4.0		ns
t_{PHL}, High to low Level Output					5.0			5.0		ns
t_{PLH}, Low to high Level Output		W			4.0			4.0		ns
t_{PHL}, High to low Level Output					5.0			5.0		ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

Logic Diagram



National Semiconductor

Preliminary

DM54ALS153/DM74ALS153 Dual 4-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Strobe inputs and a non-inverting output buffer. The Strobe inputs, when at the high level, disable their associated data inputs and force the corresponding output to the low state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

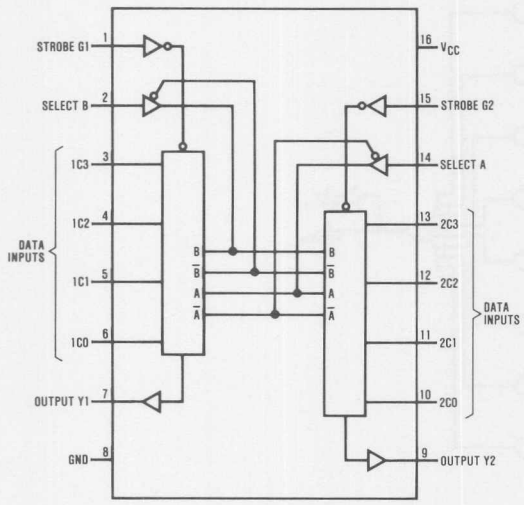
Features

- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL process.
- Switching Performance is Guaranteed Over Full Temperature and V_{CC} Supply Range.
- Pin and Functional Compatible with LS Family Counterpart.
- Improved Output Transient Handling Capability.

Absolute Maximum Ratings

Supply Voltage	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54ALS153	−55°C to 125°C
DM74ALS153	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Connection Diagram



54ALS153 (J) 74ALS153 (J,N)

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections
H = High Level L = Low Level X = Don't Care

Recommended Operating Conditions

Parameter	DM54ALS153			DM74ALS153			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

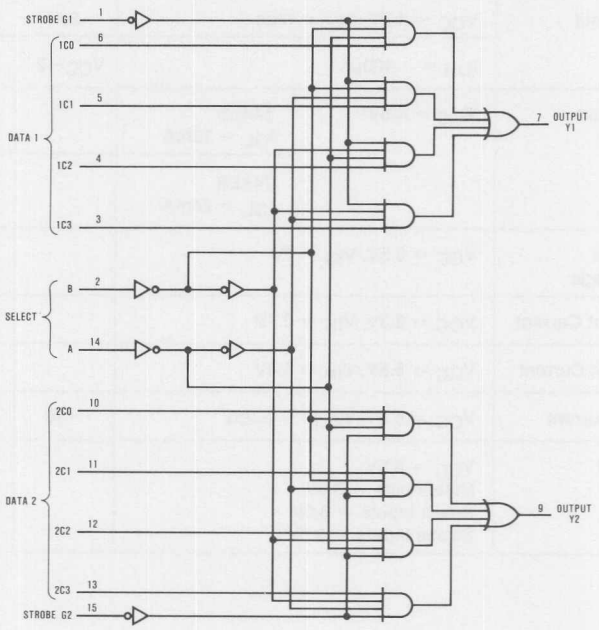
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −400μA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54ALS I_{OL} = 12mA		.25	.40	V
			74ALS I_{OL} = 24mA		.35	.50	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−200	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V Date Inputs = 3.0V Select Inputs = 3.0V Strobe Inputs = 3.0V			6.3	10	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS153			DM74ALS153			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω		7.5			7.5		ns
t_{PHL}, High to low Level Output					9.0			9.0		ns
t_{PLH}, Low to high Level Output	Data	Y			4.0			4.0		ns
t_{PHL}, High to low Level Output					6.0			6.0		ns
t_{PLH}, Low to high Level Output	Strobe	Y			4.0			4.0		ns
t_{PHL}, High to low Level Output					5.0			5.0		ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

Logic Diagram



Preliminary

National Semiconductor

DM54ALS/DM74ALS157,158 Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The ALS 157 presents true data whereas the ALS 158 presents inverted data to minimize propagation delay time.

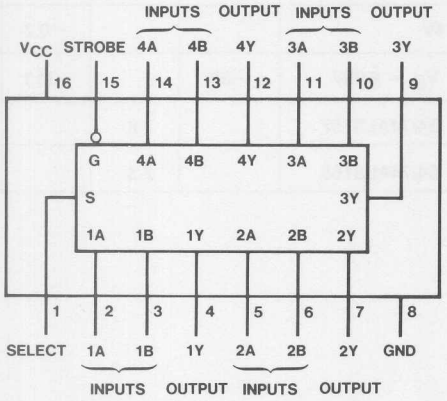
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.
- Expand any data input point.
- Multiplex dual data buses.
- General four functions of two variables (one variable is common).
- Source programmable counters.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS157 (J) **74ALS157 (J,N)**

54ALS158 (J) **74ALS158 (J,N)**

Function Table

Inputs				Output Y	
Strobe	Select	A	B	ALS157	ALS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care

1

Recommended Operating Conditions

Parameter	DM54ALS157,158			DM74ALS157,158			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

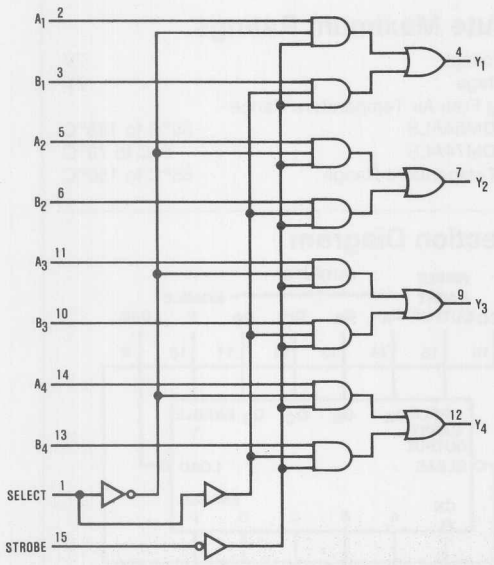
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	54/74ALS157		7.8		mA
			54/74ALS158		2.3		mA

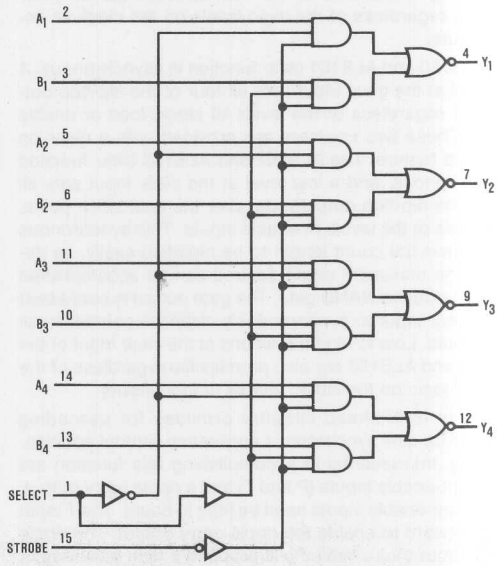
Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		From (Input)	To (Output)	Conditions	DM54ALS157,158			DM74ALS157,158			Unit
					Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation Delay Time. Low to High Level Output	157	Data	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	1.7	3.5	8.7	1.7	3.5	7.0	ns
	158				1.7	3.5	8.7	1.7	3.5	7.0	
T_{PHL}, Propagation Delay Time. High to Low Level Output	157				2.5	5.0	12.5	2.5	5.0	10.0	
	158				2.5	5.0	12.5	2.5	5.0	10.0	
T_{PLH}, Propagation Delay Time. Low to High Level Output	157	Strobe	Y		3.0	6.0	15.0	3.0	6.0	12.0	
	158				3.0	6.0	15.0	3.0	6.0	12.0	
T_{PHL}, Propagation Delay Time. High to Low Level Output	157				3.2	6.5	16.2	3.2	6.5	13.0	
	158				3.1	6.2	15.5	3.1	6.2	12.4	
T_{PLH}, Propagation Delay Time. Low to High Level Output	157	Select	Y		3.0	6.0	15.0	3.0	6.0	12.0	
	158				3.0	6.0	15.0	3.0	6.0	12.0	
T_{PHL}, Propagation Delay Time. High to Low Level Output	157				3.2	6.5	16.2	3.2	6.5	13.0	
	158				3.1	6.2	15.5	3.1	6.2	12.4	

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

Logic Diagrams





1

National Semiconductor

Preliminary

DM54ALS/DM74ALS160,161,162,163 Synchronous Four-Bit Counters

General Description

These synchronous presettable counters feature an internal carry look ahead for application in high speed counting designs. The ALS160 and ALS162 are four-bit decade counters, while the ALS161 and ALS163 are four-bit binary counters. The ALS160 and ALS161 clear asynchronously, while the ALS162 and ALS163 clear synchronously. The carry output is decoded to preveht spikes during normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable, that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with set up data after the next clock pulse regardless of the levels of enable input. Low to high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs.

The ALS160 and ALS161 clear function is asynchronous. A low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs. These two counters are provided with a clear on power-up feature. The ALS162 and ALS163 clear function is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. Low to high transitions at the clear input of the ALS162 and ALS163 are also permissible regardless of the levels of logic on the clock, enable or load inputs.

The carry look ahead circuitry provides for cascading counters for n bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs (P and T) and a ripple carry output. Both count-enable inputs must be high to count. The T input is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high level output pulse with a duration approximately equal to the high level portion of QA output. This high level overflow ripple carry pulse can be used to enable successive cascaded stages. High to low level transitions at the enable P or T inputs of the ALS160 through ALS163, may occur regardless of the logic level on the clock.

The ALS160 through ALS163 feature a fully independent clock circuit. Changes made to control inputs (enable P or T, or load) that will modify the operating mode will have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

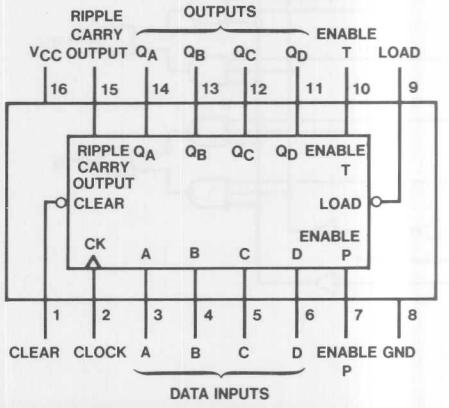
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Shottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.
- Synchronously programmable.
- Internal look ahead for fast counting.
- Carry output for n-bit cascading.
- Synchronous counting.
- Load control line.
- ESD inputs.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS160 (J) **74ALS160 (J,N)**
54ALS161 (J) **74ALS161 (J,N)**
54ALS162 (J) **74ALS162 (J,N)**
54ALS163 (J) **74ALS163 (J,N)**

Recommended Operating Conditions

Parameter		DM54ALS 160,161,162,163			DM74ALS 160,161,162,163			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−0.4			−0.4	mA
Low Level Output Current, I_{OL}				4			8	mA
Clock Frequency, f_{CLOCK}		0		50	0		55	MHz
tsetup, Set-up time	Data; A, B, C, D	12	6		12	6		ns
	En P, En T	16	8		16	8		ns
	Load	16	8		16	8		ns
	Clear (Only for 162 & 163)	20	10		20	10		ns
Set-up 1 (Only for 160 & 161)	Clear	8	4		8	4		ns
thold, Hold time	Data; A, B, C, D	0	−3		0	−3		ns
	En P, En T	0	−3		0	−3		ns
	Load	0	−4		0	−4		ns
	Clear (Only for 162 & 163)	0	−7		0	−7		ns
Hold 0 (Only for 160 & 161)	Clear	0	−4		0	−4		ns
Width of Clock or Clear Pulse, T_W		10			9			ns

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4mA		0.25	0.4	V
			74ALS I_{OL} = 8mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V	DATA, CLR, CLK, EN P LOAD, EN T			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V DATA, CLR, CLK, EN P, LOAD, ENT				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}		V_{CC} = 5.5V			11	16	mA

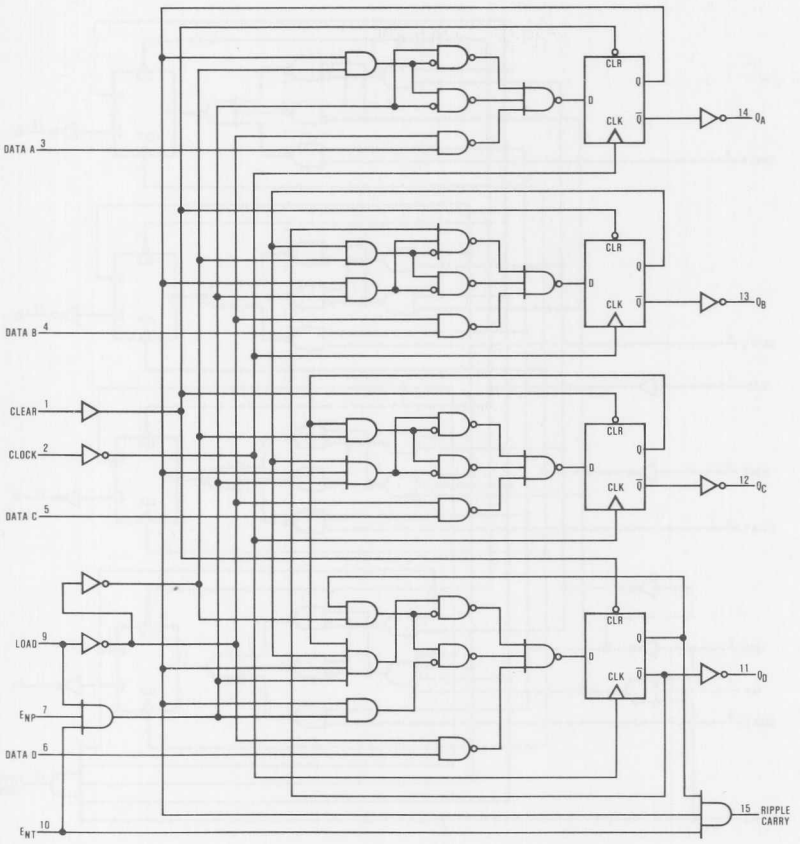
Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS 160, 161, 162, 163			DM74ALS 160, 161, 162, 163			Unit
				Min	Typ	Max	Min	Typ	Max	
fmax, Max. clock freq.			V_{CC} = 4.5 to 5.5V R_L = 500 Ω C_L = 50 pF	50	90		55	90		MHZ
T_{PLH}, Propagation delay time. Low to high level output.	Clock	Ripple Carry		4	14	25	4	14	23	ns
T_{PHL}, Propagation delay time. High to low level output. With Load High				3	10	18	3	10	17	ns
With Load Low				5	15	27	5	15	25	ns
T_{PLH}, Propagation delay time. Low to high level output.	Clock	Any Q		3	9	16	3	9	15	ns
T_{PHL}, Propagation delay time. High to low level output.				3	10	19	3	10	17	ns
T_{PLH}, Propagation delay time. Low to high level output.	En T	Ripple Carry		2	5	9	2	5	8	ns
T_{PHL}, Propagation delay time. Low to high level output.				2	6	11	2	6	10	ns
T_{PHL}, Propagation delay time. High to low level output.	Clear	Any Q		4	12	22	4	12	20	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-3.

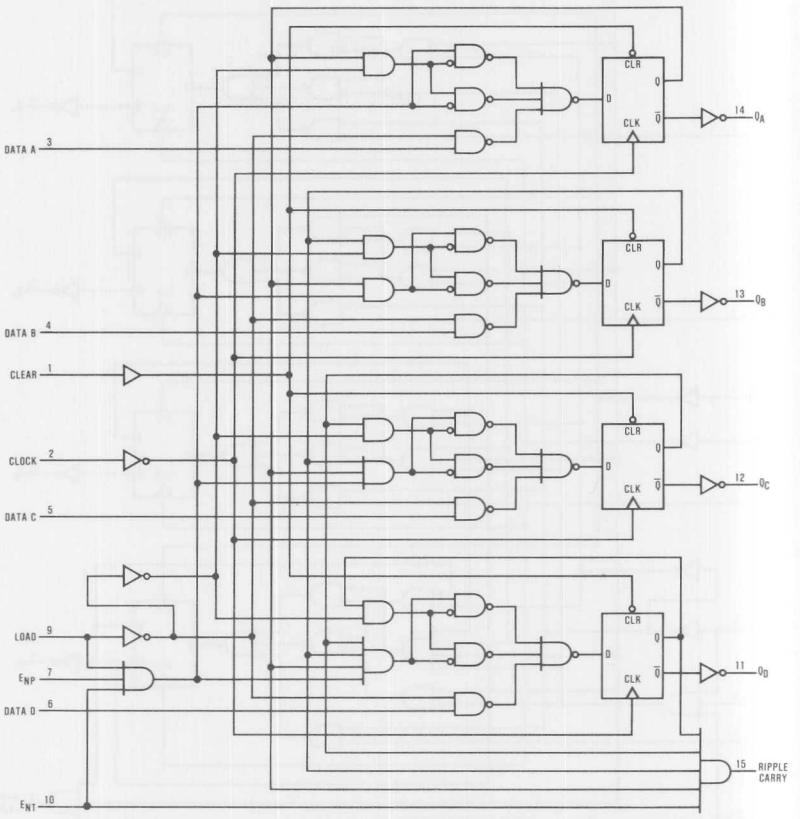
Logic Diagrams

ALS160



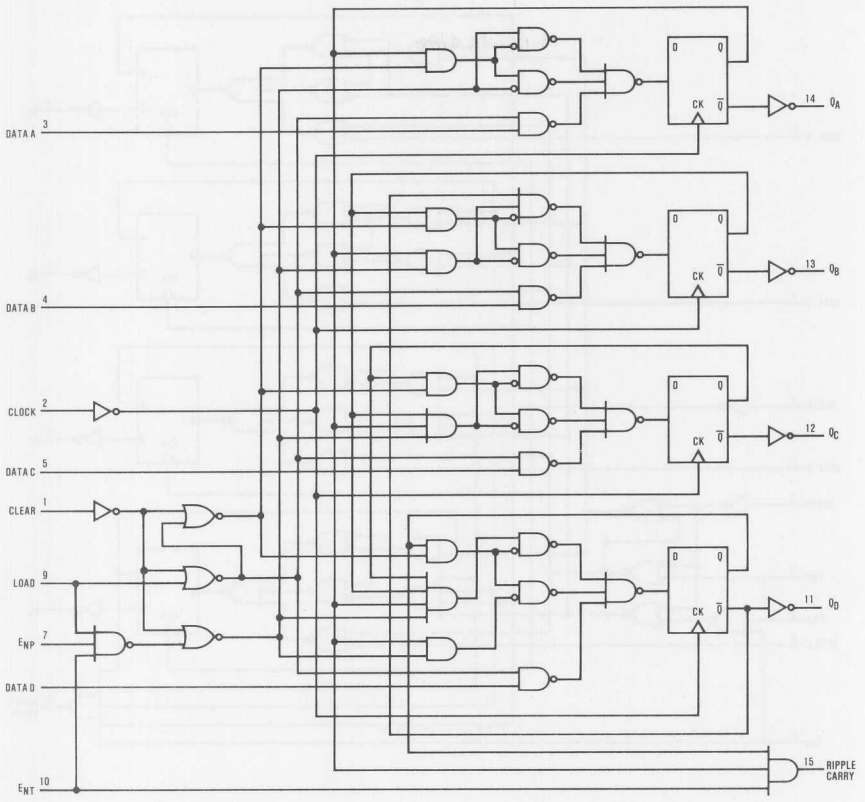
Logic Diagrams

ALS161



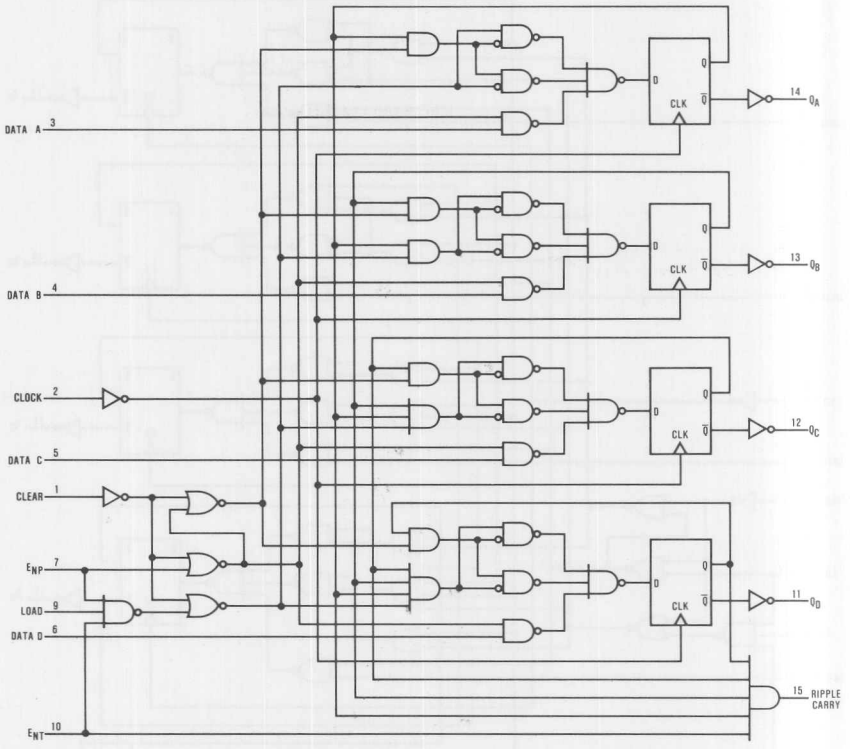
Logic Diagrams

ALS162



Logic Diagrams

ALS163



National Semiconductor

Preliminary

DM54ALS/DM74ALS168,169
Synchronous Four Bit Up/Down Counters

General Description

These synchronous presettable counters feature an internal carry look ahead for cascading in high speed counting applications. The ALS168 is a four-bit decade up/down counter and the ALS169 is a four-bit binary up/down counter. The carry output is decoded to prevent spikes during normal mode of counting operation. Synchronous operation is provided so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive going) edge of clock input waveform.

These counters are fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry outputs. The carry output thus enabled will produce a low level output pulse with a duration approximately equal to the high portion of the QA output when counting up, and approximately equal to the low portion of the QA output when counting down. This low level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input.

The control functions for these counters are fully synchronous. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) which modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

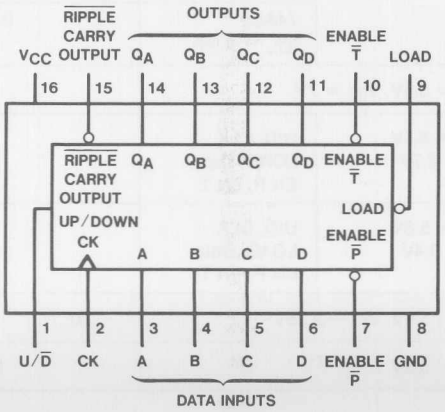
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-for-Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.
- Synchronously Programmable.
- Internal Look Ahead for Fast Counting.
- Carry Output for N-bit Cascading.
- Synchronous Counting.
- Load Control Line.
- ESD Inputs.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS168 (J) **74ALS168 (J,N)**

54ALS169 (J) **74ALS169 (J,N)**

Recommended Operating Conditions

Parameter		DM54ALS168,168			DM74ALS168,169			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−0.4			−0.4	mA
Low Level Output Current, I_{OL}				4			8	mA
Clock Frequency, f_{CLOCK}		0		50	0		55	MHz
tsetup, Set-up time	Data; A, B, C, D	12	6		12	6		ns
	En $\overline{P}$, En $\overline{T}$	16	8		16	8		ns
	Load	16	8		16	8		ns
	U/$\overline{D}$	20	10		20	10		ns
thold, Hold time	Data; A, B, C, D	0	−3		0	−3		ns
	En $\overline{P}$, En $\overline{T}$	0	−3		0	−3		ns
	Load	0	−4		0	−4		ns
	U/$\overline{D}$	0	−4		0	−4		ns
Width of Clock Pulse, T_W		10			9			ns

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

Parameters		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −.4mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 5.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 4.5V V_{IH} = 2.7V	U/$\overline{D}$, CLK, LOAD, Data, EN $\overline{P}$, EN $\overline{T}$			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V	U/$\overline{D}$, CLK, LOAD, Data, EN $\overline{P}$, EN $\overline{T}$			−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−110	mA
I_{CC}		V_{CC} = 5.5V			13	20	mA

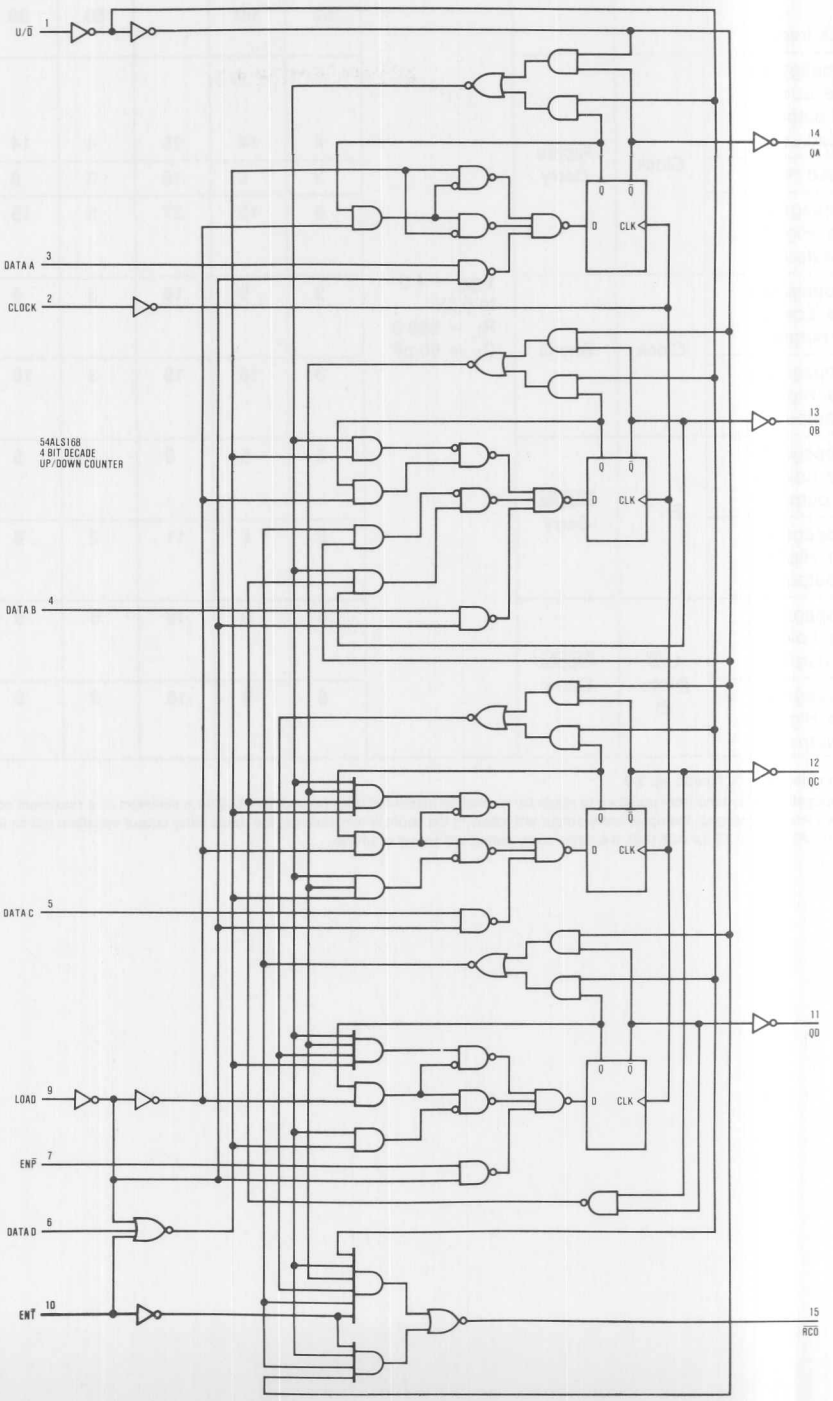
Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS168,169			DM74ALS168,169			Unit
				Min	Typ	Max	Min	Typ	Max	
fmax, Max. clock freq.			V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF	50	90		50	90		MHz
T_{PLH}, Propagation delay time. Low to high level output. With Load Low	Clock	$\overline{\text{Ripple}}$ Carry		4	14	25	4	14	23	ns
With Load High				3	8	16	3	8	14	ns
T_{PHL}, Propagation delay time. High to low level output.				5	15	27	5	15	25	ns
T_{PLH}, Propagation delay time. Low to high level output.	Clock	Any Q		3	9	16	3	9	15	ns
T_{PHL}, Propagation delay time. High to low level output.				3	10	19	3	10	17	ns
T_{PLH}, Propagation delay time. Low to high level output.	En T	$\overline{\text{Ripple}}$ Carry		2	5	9	2	5	8	ns
T_{PHL}, Propagation delay time. High to low level output.				2	6	11	2	6	10	ns
T_{PLH}, Propagation delay time. Low to high level output.	U/$\overline{\text{D}}$ (Note 2)	$\overline{\text{Ripple}}$ Carry		6	9	18	6	9	16	ns
T_{PHL}, Propagation delay time. High to low level output.				6	9	18	6	9	16	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-3.

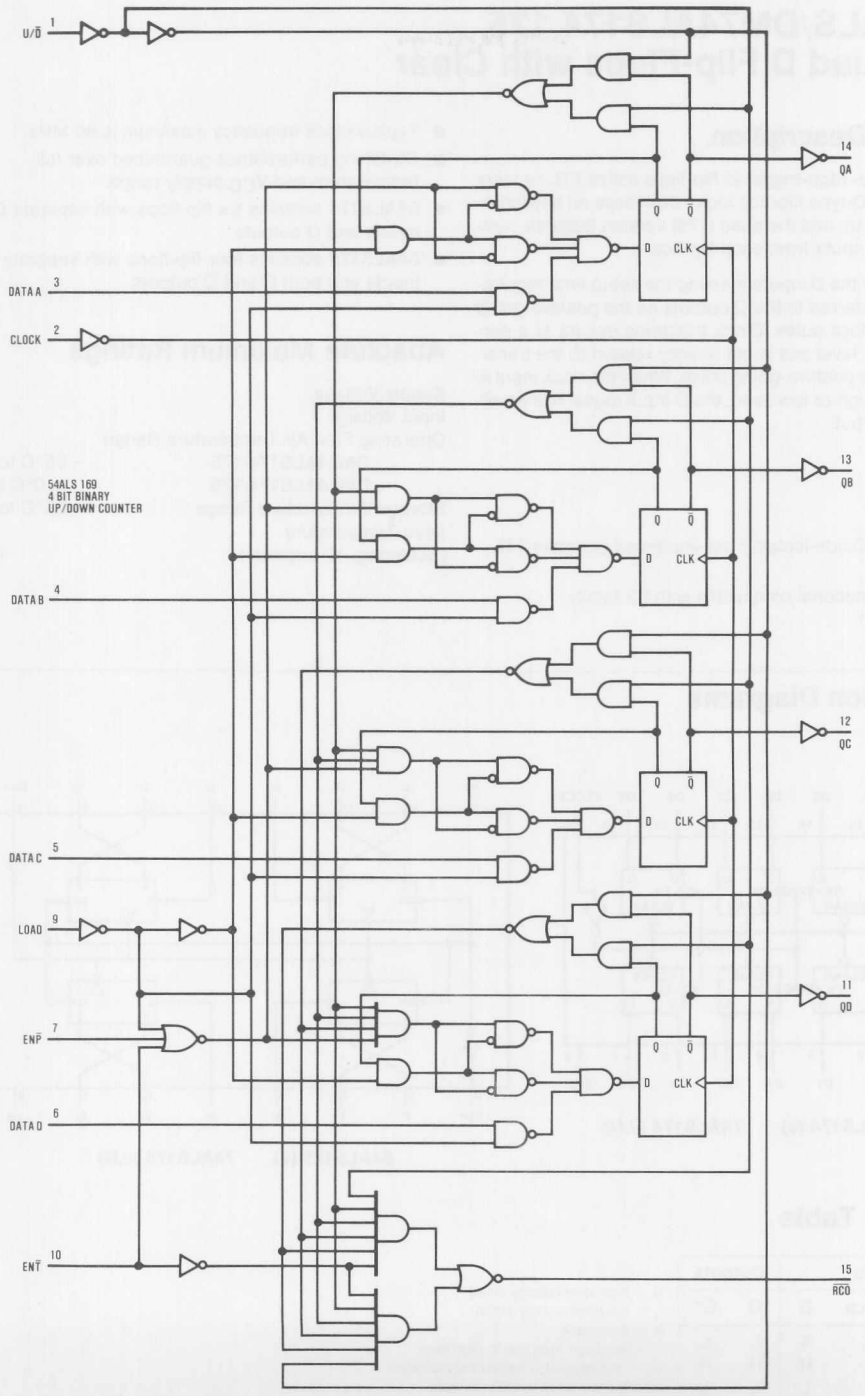
NOTE 2: Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for ALS168 or 15 for ALS169), the ripple carry output will be out of phase.

Logic Diagram



DM54ALS/DM74ALS168

Logic Diagram



DM54ALS/DM74ALS169

National Semiconductor

Preliminary

DM54ALS/DM74ALS174,175
Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. Both have an asynchronous clear input, and the quad (175) version features complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

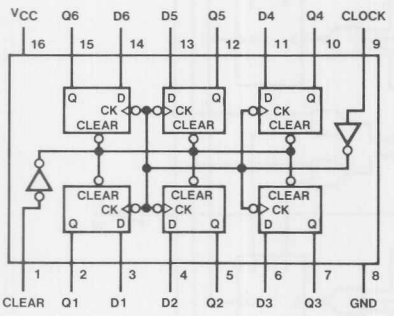
Features

- Advanced Oxide-Isolated Ion-Implanted Schottky TTL Process.
- Pin and Functional compatible with LS family counterpart.
- Typical clock frequency maximum is 80 MHz.
- Switching performance guaranteed over full temperature and V_{CC} supply range.
- 54ALS174 contains six flip-flops with separate D inputs and Q outputs.
- 54ALS175 contains four flip-flops with separate D inputs and both Q and $\overline{Q}$ outputs.

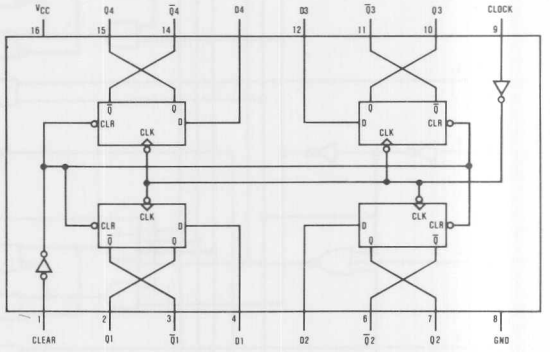
Absolute Maximum Ratings

Supply Voltage	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54ALS174/175	−55°C to 125°C
DM74ALS174/175	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Connection Diagrams



54ALS174 (J) 74ALS174 (J,N)



54ALS175 (J) 74ALS175 (J,N)

Function Table

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$*
L	X	X	L	L
H	↑	H	H	H
H	↑	L	L	L
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = don't care
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
* applies to 54ALS175/74ALS175 only

Recommended Operating Conditions

Parameter	DM54ALS174,175			DM74ALS174,175			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−400			−400	mA
Low Level Output Current, I_{OL}			4			8	mA
Pulse Width, t_W Clock							ns
Clear							
Setup Time, t_{SETUP} Data Input							ns
Clear Inactive State							
Hold Time, t_{HOLD} Data Input	0			0			ns
Clear Active State	0			0			

Electrical Characteristics over recommended operating free air temperature range (Note 1)

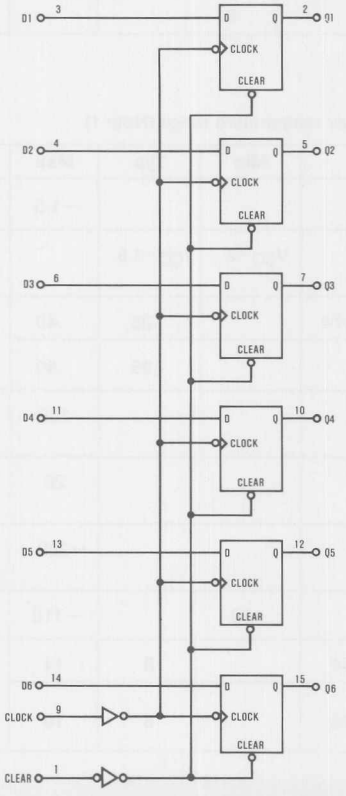
	Parameter	Conditions			Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_{IN} = −18mA					−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V I_{OH} = −400μA			V_{CC}−2	V_{CC}−1.6		V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	I_{OL} = 4mA	DM54/74		.25	.40	V
			I_{OL} = 8mA	DM74		.35	.50	
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V					100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V					−200	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V = 2.25V			−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V Clock = 3.0V Clear = .4V D Inputs = 3.0V		ALS174		8	14	mA
				ALS175		6	10	

Switching Characteristics over recommended operating free air temperature range (Note 1)

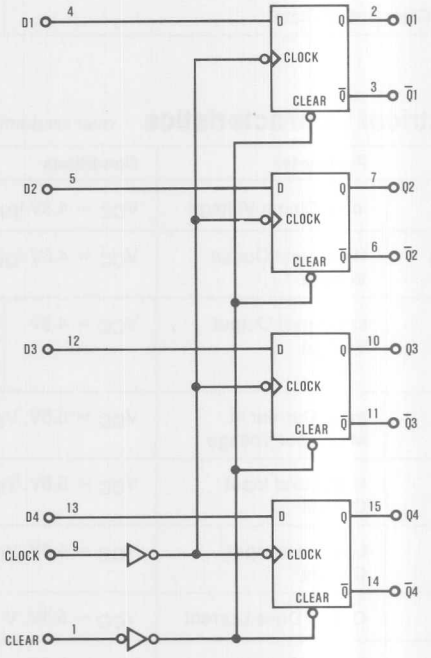
Parameter	Conditions	54ALS174,175			74ALS174,175			Unit
		Min	Typ	Max	Min	Typ	Max	
f_{MAX}, Maximum Clock Frequency	R_L = 500Ω C_L = 50pF		80			80		MHz
t_{PLH}, Propagation Delay Time, Low to high Level Output From Clear (175 Only)	R_L = 500 Ω C_L = 50pF		10			10		ns
t_{PHL}, Propagation Delay Time, High to low Level Output From Clear	R_L = 500 Ω C_L = 50pF		11			11		ns
t_{PLH}, Propagation Delay Time, Low to high Level Output From Clock	R_L = 500 Ω C_L = 50pF		9			9		ns
t_{PHL}, Propagation Delay Time, High to low Level Output From Clock	R_L = 500 Ω C_L = 50pF		10			10		ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-3.

Logic Diagrams



54ALS174/74ALS174



54ALS175/74ALS175

Preliminary

National Semiconductor

DM54ALS/DM74ALS240,241,242,243,244 TRI-STATE® Bus Drivers/Receivers

General Description

This family of Advance Low Power Schottky TRI-STATE Bus circuits are designed to provide either bidirectional or unidirectional buffer interface in Memory, Microprocessor, and Communication Systems. The output characteristics of the circuits have low impedance sufficient to drive terminated transmission lines down to 133 ohms. The input characteristics of the circuits likewise have a high impedance so it will not significantly load the transmission line. The package contains eight TRI-STATE buffers organized with four buffers having a common TRI-STATE enable gate. The ALS240, 241 and 244 are eight wide in a 20 pin package, and may be used as a 4 wide bidirectional or eight wide unidirectional. The ALS242 and 243 are organized four wide bidirectional in a 14 pin package. The buffer selection includes inverting and non-inverting, with enable or disable TRI-STATE control. The TRI-STATE circuitry contains a feature that maintains the buffers in TRI-STATE until the power supply (V_{CC}) is greater than 3V. This feature prevents the buffers from glitching the system bus during power up or down.

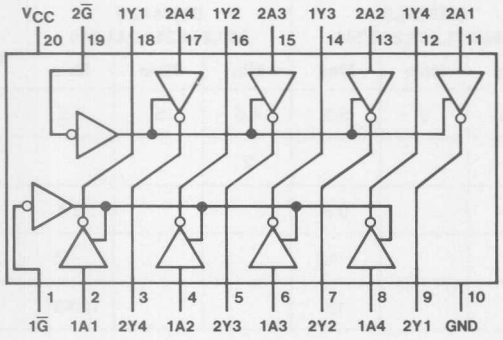
Features

- Advanced Low Power Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Switching Performance with Less Power Dissipation compared with 54/74ALS Counterpart.
- Functional and Pin Compatible with 54/74LS Counterpart.
- Switching Response Specified Into 500 ohm and 50pF.
- Low Level Drive Current
  74ALS-1 48ma , 74ALS 24ma , 54ALS 12ma
- Glitch Free Bus During Power Up/Down.
- Specified to Interface with CMOS at
  $V_{OH} = V_{CC} - 2V$.

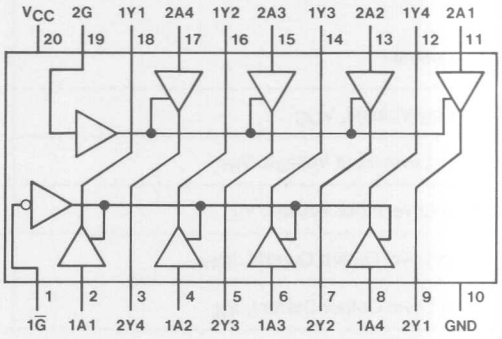
Absolute Maximum Ratings

Supply Voltage, V_{CC}	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
(Soldering, 10 seconds)	+300°C

Connection Diagrams

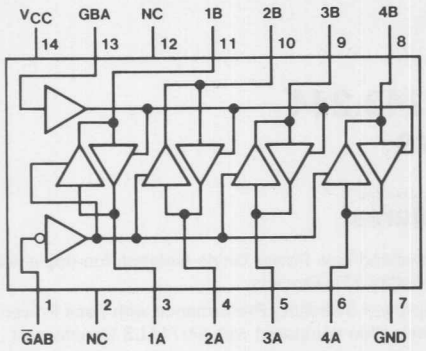


54ALS240 (J) 74ALS240 (J,N)

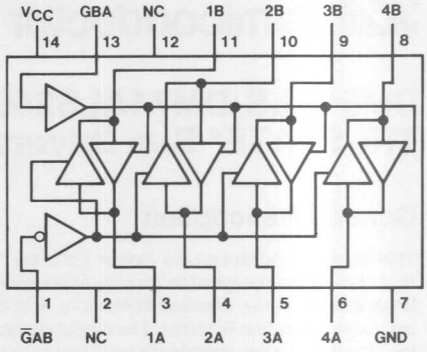


54ALS241 (J) 74ALS241 (J,N)

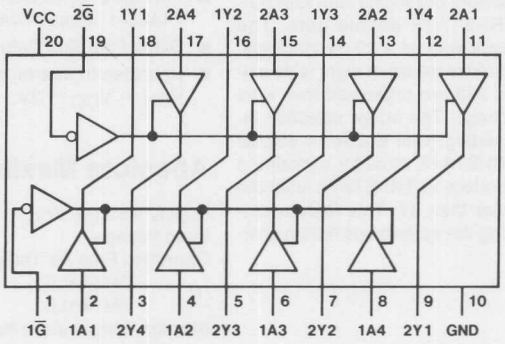
Connection Diagrams



54ALS242 (J) 74ALS242 (J,N)



54ALS243 (J) 74ALS243 (J,N)



54ALS244 (J) 74ALS244 (J,N)

Recommended Operating Conditions

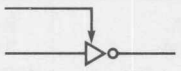
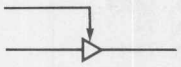
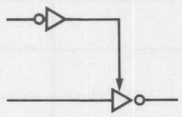
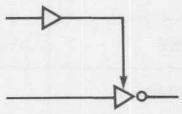
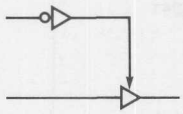
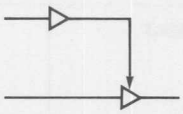
Parameter	DM54ALS 240,241,242,243,244			DM74ALS 240,241,242,243,244			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			12			12/48*	mA

* Applies to 74ALS-1 options.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions	Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = −3mA V_{CC} = 4.5V, I_{OH} = −15mA I_{OH} = −400μA	2.4 2.0 V_{CC}−2	3.2 2.3		V V V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = 12mA 54/74 I_{OL} = 24mA 74 I_{OL} = 48mA 74-1		.25 .35 .35	.40 .50 .50	V V V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V			100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V			−200	μA
I_{OZH}	High Level TRI-STATE® Output Current	V_{CC} = 5.5V, V = 2.7V			20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V = .4V			−20	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V 54/74ALS240 Outputs High Outputs Low TRI-STATE		 4.7 10.6 11.7		mA
I_{CC}	Supply Current	V_{CC} = 5.5V 54/74ALS241 Outputs High Outputs Low TRI-STATE		 8.0 13.9 15.1		mA
I_{CC}	Supply Current	V_{CC} = 5.5V 54/74ALS242 A Port Outputs High A Port Outputs Low TRI-STATE				mA
I_{CC}	Supply Current	V_{CC} = 5.5V 54/74ALS243 A Port Outputs High A Port Outputs Low TRI-STATE				mA
I_{CC}	Supply Current	V_{CC} = 5.5V 54/74ALS244 Outputs High Outputs Low TRI-STATE		 7.6 13.5 14.8		mA

Switching Characteristics over recommended operating free air temperature range (Notes 1, 2)

Parameter (Propagation Delay Time)	Circuit Configuration	74ALS			54ALS			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Low-to-High Level Output			3.2			3.2		ns
T_{PHL}, High-to-Low Level Output	ALS 240, 242		2.0			2.0		ns
T_{PLH}, Low-to-High Level Output			4.0			4.0		ns
T_{PHL}, High-to-Low Level Output	ALS 241, 243, 244		4.5			4.5		ns
T_{PZL}, Output Enable to Low Level			7.2			7.2		ns
T_{PZH}, Output Enable to High Level			5.5			5.5		ns
T_{PLZ}, Output Disable From Low Level			4.5			4.5		ns
T_{PHZ}, Output Disable From High Level	ALS 240, 242		3.5			3.5		ns
T_{PZL}, Output Enable to Low Level			9.2			9.2		ns
T_{PZH}, Output Enable to High Level			7.0			7.0		ns
T_{PLZ}, Output Disable From Low Level			5.0			5.0		ns
T_{PHZ}, Output Disable From High Level	ALS 242		3.5			3.5		ns
T_{PZL}, Output Enable to Low Level			8.5			8.5		ns
T_{PZH}, Output Enable to High Level			6.2			6.2		ns
T_{PLZ}, Output Disable From Low Level			5.0			5.0		ns
T_{PHZ}, Output Disable From High Level	ALS 241, 243, 244		3.5			3.5		ns
T_{PZL}, Output Enable to Low Level			9.2			9.2		ns
T_{PZH}, Output Enable to High Level			7.0			7.0		ns
T_{PLZ}, Output Disable From Low Level			5.0			5.0		ns
T_{PHZ}, Output Disable From High Level	ALS 241, 242		3.5			3.5		ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-2.

NOTE 2: Switching characteristic conditions are V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50pF

Preliminary

National Semiconductor

DM54ALS251/DM74ALS251 TRI-STATE® 8-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-eight data sources as a result of a unique three-bit binary code at the Select inputs. Two complementary outputs provide both inverting and non-inverting buffer operation. An Output Control input is provided which, when at the high level, places both outputs in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

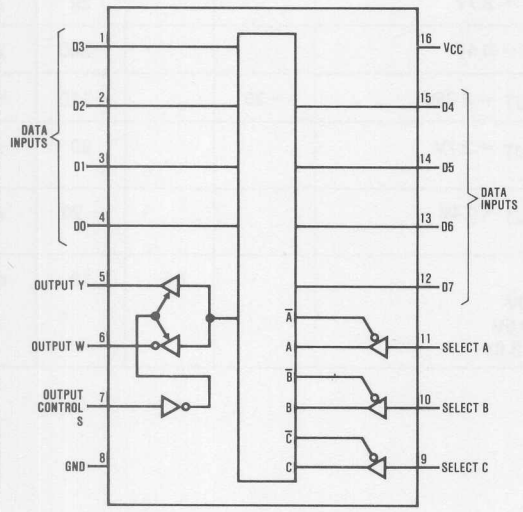
Features

- Advanced Oxide-Isolated Ion-Implanted Schottky TTL Process.
- Switching Performance is Guaranteed Over Full Temperature and V_{CC} Supply Range.
- Pin and Functional Compatible with LS Family Counterpart.
- Improved Output Transient Handling Capability.
- Output Control Circuitry Incorporates Power-Up Tri-State Feature.

Absolute Maximum Ratings

Supply Voltage, V_{CC}	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54ALS251	−55°C to 125°C
DM74ALS251	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Connection Diagram



54ALS251 (J) 74ALS251 (J,N)

Function Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Logic Level, L = Low Logic Level, X = Don't Care
Z = High Impedance (Off)
D0 thru D7 = The Level of the Respective D Input

1

Recommended Operating Conditions

Parameter	DM54ALS251			DM74ALS251			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

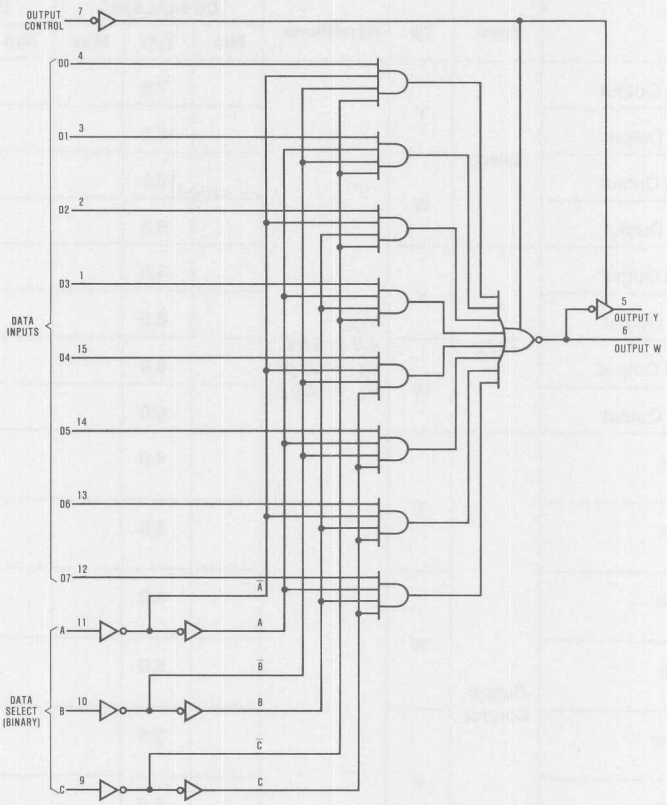
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = 400 μA		V_{CC}-2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54ALS/74ALS I_{OL} = 12mA		.25	.40	V
			74ALS I_{OL} = 24mA		.35	.50	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−200	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Bias	V_{CC} = 5.5V, V_{OUT} = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Bias	V_{CC} = 5.5V, V_{OUT} = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Data Inputs = 3.0V Select Inputs = 3.0V Control Inputs = 3.0V			7.5	12	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS251			DM74ALS251			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω		7.5			7.5		ns
t_{PHL}, High to low Level Output					10.5			10.5		ns
t_{PLH}, Low to high Level Output		W			10.5			10.5		ns
t_{PHL}, High to low Level Output					9.5			9.5		ns
t_{PLH}, Low to high Level Output	Data	Y			4.0			4.0		ns
t_{PHL}, High to low Level Output					6.0			6.0		ns
t_{PLH}, Low to high Level Output		W			6.0			6.0		ns
t_{PHL}, High to low Level Output					6.0			6.0		ns
t_{ZH}, Output Enable Time to High Level	Output Control	Y			4.0			4.0		ns
t_{ZL}, Output Enable Time to Low Level					5.0			5.0		ns
t_{ZH}, Output Enable Time to High Level		W			4.0			4.0		ns
t_{ZL}, Output Enable Time to Low Level					5.0			5.0		ns
t_{HZ}, Output Disable Time From High Level		Y			3.5			3.5		ns
t_{LZ}, Output Disable Time From Low Level					5.0			5.0		ns
t_{HZ}, Output Disable Time From High Level		W			3.5			3.5		ns
t_{LZ}, Output Disable Time From Low Level					5.0			5.0		ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-2.

Logic Diagram



Preliminary

National Semiconductor

DM54ALS253/DM74ALS253 TRI-STATE® Dual 4-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select Inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Output Control inputs and a non-inverting Tri-state output buffer. The Output Control inputs, when at the high level, place the corresponding output in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

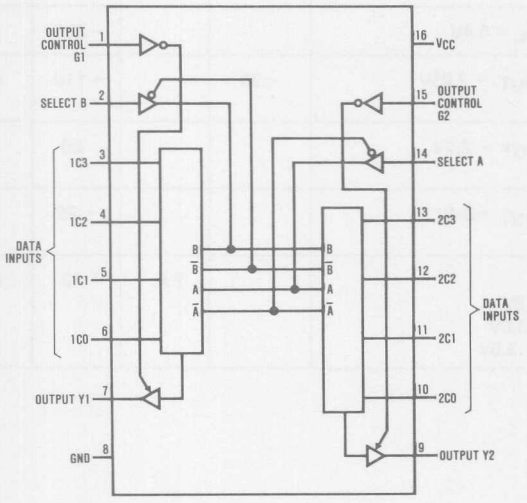
Features

- Advanced Oxide-Isolated Ion-Implanted Schottky TTL Process.
- Switching Performance is Guaranteed Over Full Temperature and V_{CC} Supply Range.
- Pin and Functional Compatible with LS Family Counterpart.
- Improved Output Transient Handling Capability.
- Output Control Circuitry Incorporates Power-Up Tri-State Feature.

Absolute Maximum Ratings

Supply Voltage, V_{CC}	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54ALS253	−55°C to 125°C
DM74ALS253	0° to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Connection Diagram



54ALS253 (J) 74ALS253 (J,N)

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections

H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

Recommended Operating Conditions

Parameter	DM54ALS253			DM74ALS253			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

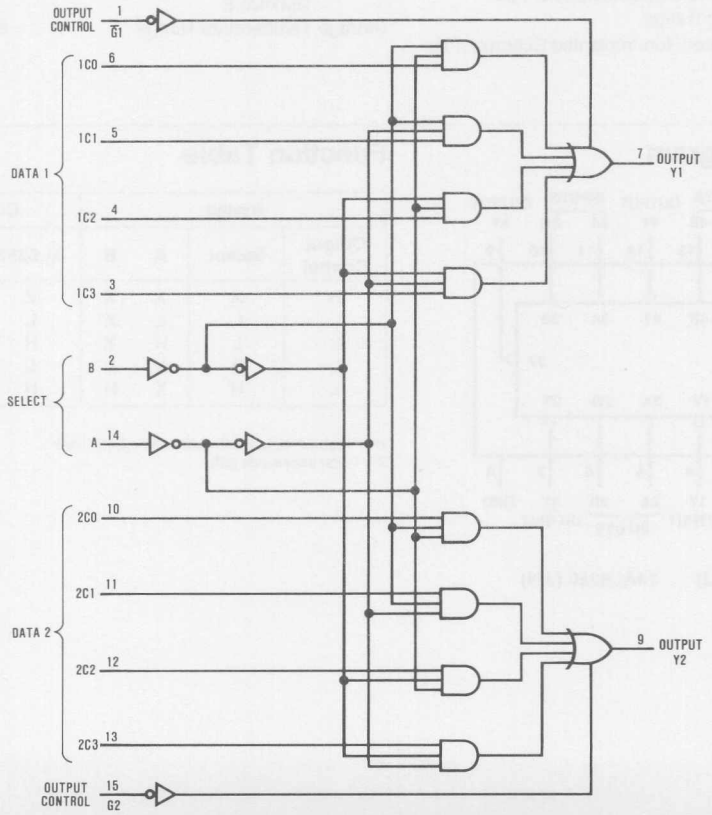
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = 400 μA		V_{CC}-2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		.25	.40	V
			74ALS I_{OL} = 24mA		.35	.50	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−200	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Bias	V_{CC} = 5.5V, v_{OUT} = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Bias	V_{CC} = 5.5V, V_{OUT} =0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Data Inputs = 3.0V Select Inputs = 3.0V Control Inputs = 3.0V			7.6	12	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS253			DM74ALS253			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V C_L = 50 pF R_L = 500 Ω		7.5			7.5		ns
t_{PHL}, High to low Level Output					9.0			9.0		ns
t_{PLH}, Low to high Level Output	Data				4.0			4.0		ns
t_{PHL}, High to low Level Output					6.0			6.0		ns
t_{ZH}, Output Enable Time to High Level	Output Control	Y			4.0			4.0		ns
t_{ZL}, Output Enable Time to Low Level					5.0			5.0		ns
t_{HZ}, Output Disable Time From High Level					4.0			4.0		ns
t_{LZ}, Output Disable Time From Low Level					5.0			5.0		ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-2.

Logic Diagram



National Semiconductor

Preliminary

DM54ALS/DM74ALS257,258 TRI-STATE® Quad 2-Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four TRI-STATE outputs that can interface directly with data lines of bus-organized systems. A 4-bit word selected from one of two sources is routed to the four outputs. The ALS257 presents true data whereas the ALS258 presents inverted data to minimize propagation delay time.

This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

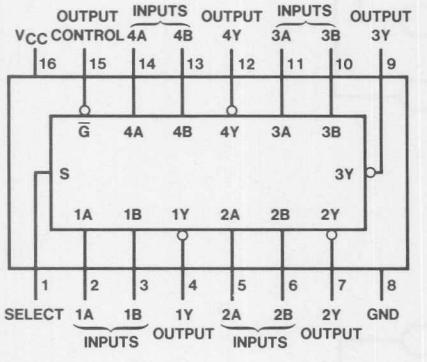
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Expand any data input point.
- Multiplex dual data buses.
- General four functions of two variables (one variable is common).
- Source programmable counters.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS258 (J) 74ALS258 (J,N)

Function Table

Inputs				Output Y	
Output Control	Select	A	B	ALS257	ALS258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care
Z = High Impedance (off)

Recommended Operating Conditions

Parameter	DM54ALS257,258			DM74ALS257,258			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

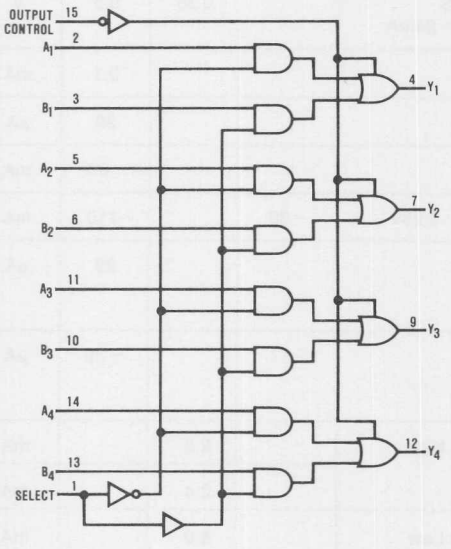
	Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage		V_{CC} = 4.5V, V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
				74ALS I_{OH} = −2.6mA	2.4	3.3		V
			I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage		V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
				74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current		V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current		V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current		V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current		V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied		V_{CC} = 5.5V V_{IH} = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_{CC} = 5.5V V_{IH} = 2V, V_O = 0.4V				−20	μA
I_{CCH}	Supply Current	ALS257	V_{CC} = 5.5V, Outputs Open	Outputs High		2.6		mA
		ALS258				2.4		mA
I_{CCL}	Supply Current	ALS257		Outputs Low		8.0		mA
		ALS258				7.0		mA
I_{CCZ}	Supply Current	ALS257		Outputs Disabled		9.3		mA
		ALS258				8.0		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

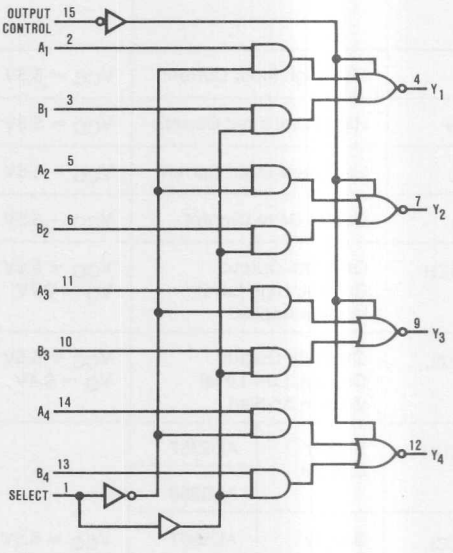
Parameter		From	To	Conditions	DM54ALS257,258			DM74ALS257,258			Unit
					Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation Delay Time. Low to high Level Output	257	Data	Any Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	1.7	3.5	8.7	1.7	3.5	7.0	ns
	258				1.7	3.5	8.7	1.7	3.5	7.0	
T_{PHL}, Propagation Delay Time. High to low Level Output	257				2.5	5.0	12.5	2.5	5.0	10.0	
	258				2.5	5.0	12.5	2.5	5.0	10.0	
T_{PLH}, Propagation Delay Time. Low to high Level Output	257	Select	Any Y		3.2	6.5	16.2	3.2	6.5	13.0	
	258				2.7	5.5	13.7	2.7	5.5	11.0	
T_{PHL}, Propagation Delay Time. High to low Level Output	257				3.5	7.0	17.5	3.5	7.0	14.0	
	258				4.0	8.0	20.0	4.0	8.0	16.0	
T_{ZH}, Output Enable Time to High Level	257	Output Control	Any Y		2.0	4.0	10.0	2.0	4.0	8.0	
	258				2.0	4.0	10.0	2.0	4.0	8.0	
T_{ZL}, Output Enable Time to Low Level	257				2.5	5.0	12.5	2.5	5.0	10.0	
	258				2.5	5.0	12.5	2.5	5.0	10.0	
T_{HZ}, Output Disable Time. From High Level	257	Output Control	Any Y		2.5	5.0	12.5	2.5	5.0	10.0	
	258				2.5	5.0	12.5	2.5	5.0	10.0	
T_{LZ}, Output Disable Time From Low Level	257				5.0	10.0	25.0	5.0	10.0	20.0	
	258				5.0	10.0	25.0	5.0	10.0	20.0	

NOTE 1: See notes pg. 1-iii, figures pg. 3-2.

Logic Diagrams



54/74ALS257



54/74ALS258

Preliminary

National Semiconductor

DM54ALS273/DM74ALS273
Octal D-Type Edge-Triggered Flip-Flops With Clear

General Description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input. The outputs are buffer type and are, thus, guaranteed at I_{OL} 12/24 mA.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

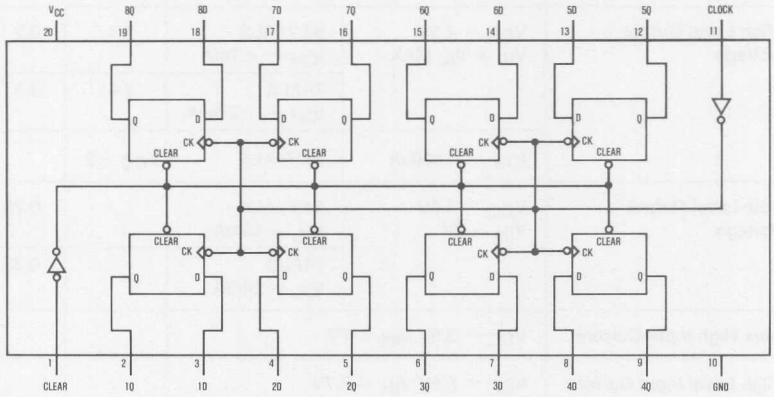
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Buffer-Type Outputs and Improved AC Offer Significant Advantage Over 'LS273.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-For-Pin Compatible with 'LS273.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS273	−55°C to 125°C
DM74ALS273	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS273 (J) **74ALS273 (J,N)**

Recommended Operating Conditions

Parameter		DM54ALS273			DM74ALS273			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−1.0			−2.6	mA
Low Level Output Current, I_{OL}				12			24	mA
Clock frequency, f_{CLOCK}		0		30	0		35	MHz
Width of Clock Pulse, T_W	High	10			10			ns
	Low	17			15			ns
Width of Clear Pulse, T_W	Low	10			10			ns
Data Setup Time, T_{SU}		10↑			10↑			ns
Data Hold Time, T_H		4↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		11	18	mA
			Outputs Low		19	29	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS273			DM74ALS273			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF.	30			35			MHz
T_{PHL}	Clear	Any Q		7		24	7		21	ns
T_{PLH}	Clock	Any Q		4		15	4		12	ns
T_{PHL}				4		15	4		12	ns

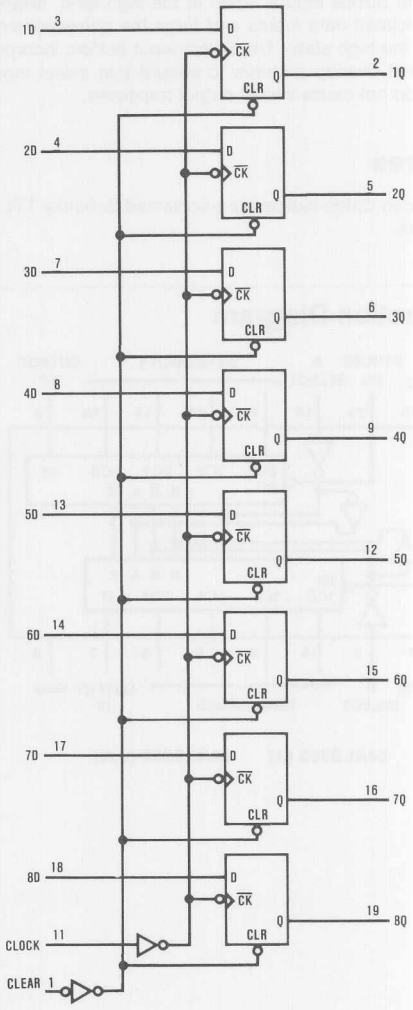
NOTE 1: See notes pg. 1-iii, figures pg. 3-3.

Function Table (Each Flip-Flop)

Inputs			Output
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition, Q_0 = Previous Condition of Q

Logic Diagram



National Semiconductor

Preliminary

DM54ALS352/DM74ALS352 Dual 4-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Strobe inputs and an inverting output buffer. The Strobe inputs, when at the high level, disable their associated data inputs and force the corresponding output to the high state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

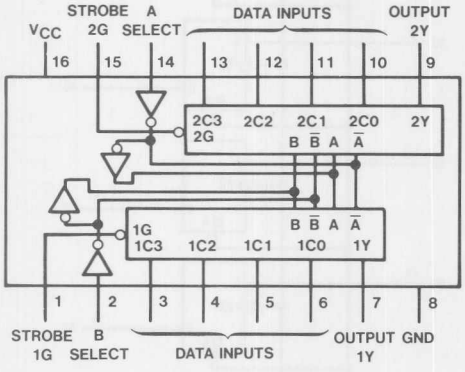
Features

- Advanced Oxide-isolated Ion-implanted Schottky TTL process.
- Switching performance is guaranteed over full temperature and V_{CC} supply range.
- Pin and functional compatible with the LS Family counterpart.
- Improved output transient handling capability.

Absolute Maximum Ratings

Supply Voltage	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54ALS352	−55°C to 125°C
DM74ALS352	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Connection Diagram



54ALS352 (J) 74ALS352 (J,N)

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections
H = High Level, L = Low Level, X = Don't Care

Recommended Operating Conditions

Parameter	DM54ALS352			DM74ALS352			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5		5.5	4.5		5.5	V
High Level Input Voltage, V_{IH}	2.0			2.0			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

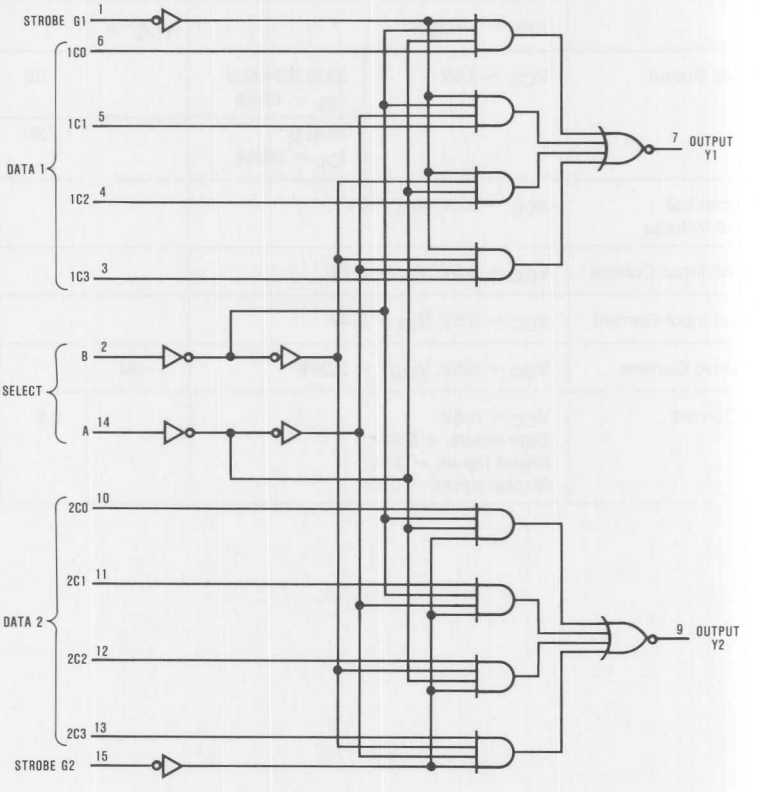
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		IOH = −400μA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54ALS/74ALS I_{OL} = 12mA		.25	.40	V
			74ALS I_{OL} = 24mA		.35	.50	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−200	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V Date Inputs = 3.0V Select Inputs = 3.0V Strobe Inputs = 0.4V			6.5	10	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS352			DM74ALS352			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω		9.0			9.0		ns
t_{PHL}, High to low Level Output					9.5			9.5		ns
t_{PLH}, Low to high Level Output	Data				6.0			6.0		ns
t_{PHL}, High to low Level Output					6.0			6.0		ns
t_{PLH}, Low to high Level Output	Strobe				4.0			4.0		ns
t_{PHL}, High to low Level Output					5.0			5.0		ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

Logic Diagram



National Semiconductor

Preliminary

DM54ALS353/DM74ALS353 TRI-STATE® Dual 4-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Output Control inputs and an inverting TRI-STATE output buffer. The Output Control inputs, when at the high level, place the corresponding output in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

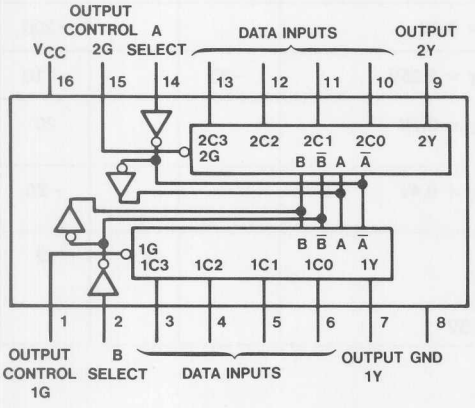
Features

- Advanced Oxide-isolated Ion-implanted Schottky TTL process.
- Switching performance is guaranteed over full temperature and V_{CC} supply range.
- Pin and functional compatible with LS Family counterpart.
- Improved output transient handling capability.
- Output Control circuitry incorporates power-up TRI-STATE feature.

Absolute Maximum Ratings

Supply Voltage	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54ALS353	−55°C to +125°C
DM74ALS353	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Connection Diagram



54ALS353 (J) 74ALS353 (J,N)

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs A and B are common to both sections
H = High Level. L = Low Level. X = Don't Care.
Z = High Impedance State

1

Recommended Operating Conditions

Parameter	DM54ALS353			DM74ALS353			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5		5.5	4.5		5.5	V
High Level Input Voltage, V_{IH}	2.0			2.0			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

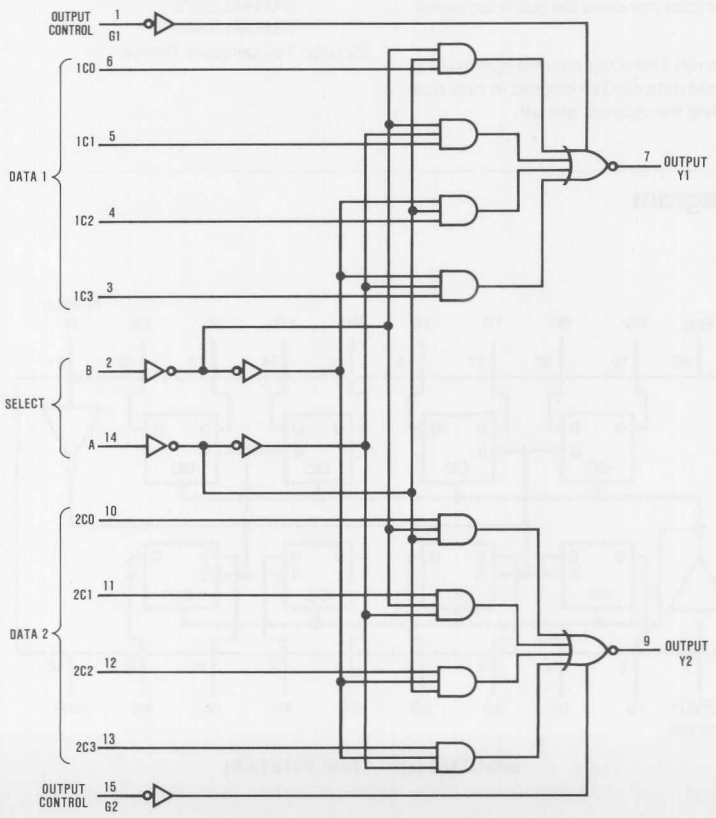
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		IOH = −400μA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54ALS/74ALS I_{OL} = 12mA		.25	.40	V
			74ALS I_{OL} = 24mA		.35	.50	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−200	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Bias	V_{CC} = 5.5V, V_{OUT} = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Bias	V_{CC} = 5.5V, V_{OUT} = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Date Inputs = 3.0V Select Inputs = 3.0V Control Inputs = 3.0V			8.0	12	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS353			DM74ALS353			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω		9.0			9.0		ns
t_{PHL}, High to low Level Output					9.5			9.5		ns
t_{PLH}, Low to high Level Output	Data				6.0			6.0		ns
t_{PHL}, High to low Level Output					6.0			6.0		ns
t_{ZH}, Output Enable Time to High Level	Output Control				4.0			4.0		ns
t_{ZL}, Output Enable Time to Low Level					5.0			5.0		ns
t_{HZ}, Output Disable Time From High Level					4.0			4.0		ns
t_{LZ}, Output Disable Time From Low Level					5.0			5.0		ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-2.

Logic Diagram



National Semiconductor

Preliminary

DM54ALS373/DM74ALS373 Octal D-Type Transparent Latches

General Description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ALS373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

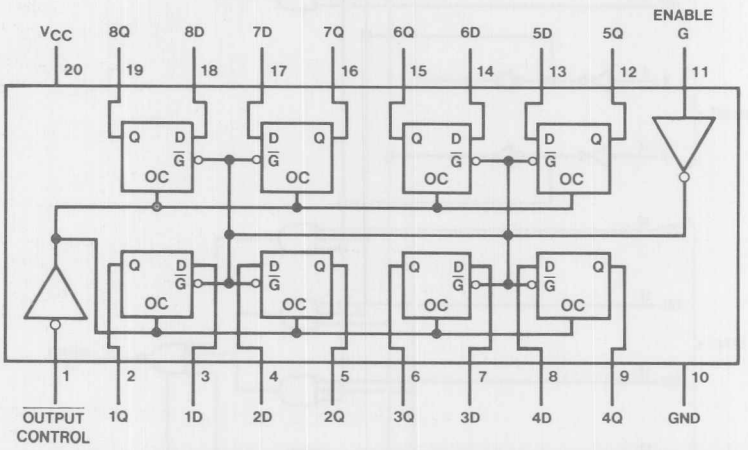
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS373 at Approximately Half the Power.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS373	−55°C to 125°C
DM74ALS373	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS373 (J) 74ALS373 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS373			DM74ALS373			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA
Width of Enable Pulse, High or Low	10			10			ns
Data Setup Time, T_{SU}	10↓			10↓			ns
Data Hold Time, T_H	7↓			7↓			ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

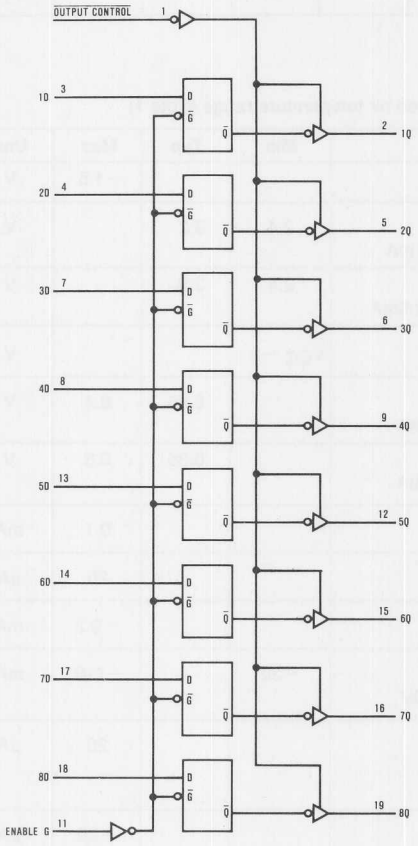
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V, V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, Outputs Open	Outputs High		9	14	mA
			Outputs Low		16	25	mA
			Outputs Disabled		17	27	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS373			DM74ALS373			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any Q	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	3		15	3		12	ns
T_{PHL}				3		15	3		12	ns
T_{PLH}	Enable	Any Q		8		25	8		20	ns
T_{PHL}				8		22	8		20	ns
T_{PZH}	Output Control	Any Q		3		18	4		15	ns
T_{PZL}				4		21	5		18	ns
T_{PHZ}				2		12	2		10	ns
T_{PLZ}				3		15	3		13	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

Logic Diagram



Function Table

$\overline{\text{Output}}$ Control	Enable G	D	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
Q_0 = Previous Condition of Q

Preliminary

National Semiconductor

DM54ALS374/DM74ALS374 Octal D-Type-Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole three-state output designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

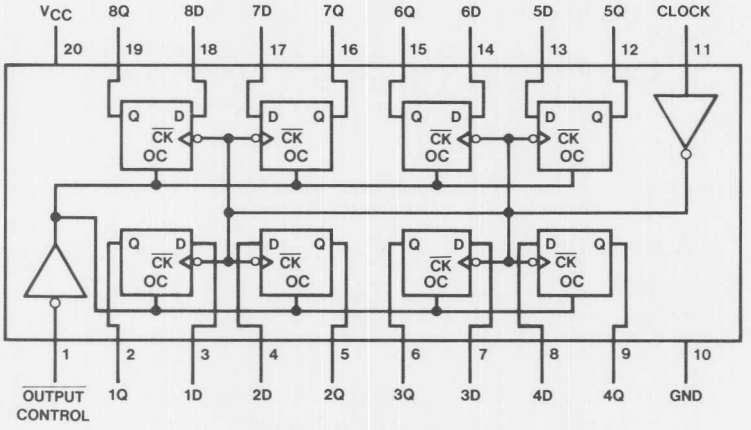
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-for-Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS374 at Approximately Half the Power.
- TRI-STATE® Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS374	−55°C to 125°C
DM74ALS374	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS374 (J) 74ALS374 (J,N)

1

Recommended Operating Conditions

Parameter		DM54ALS374			DM74ALS374			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−1.0			−2.6	mA
Low Level Output Current, I_{OL}				12			24	mA
Clock frequency, f_{CLOCK}		0		30	0		35	MHz
Width of Clock Pulse, T_W	High	10			10			ns
	Low	17			15			ns
Data Setup Time, T_{SU}		10↑			10↑			ns
Data Hold Time, T_H		4↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

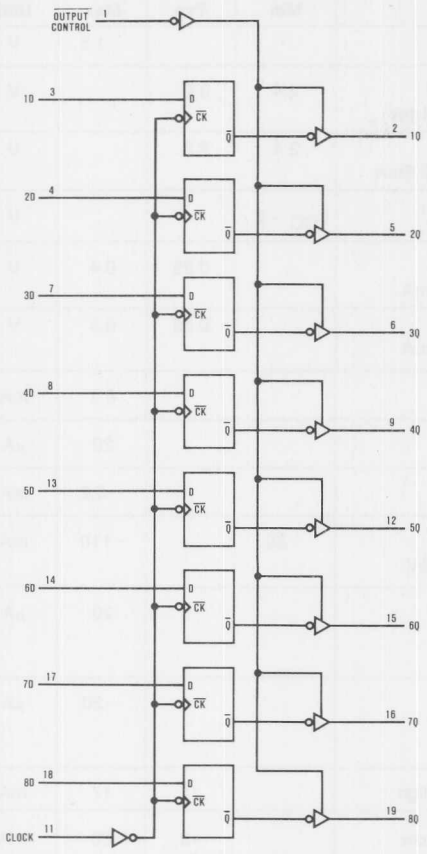
Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		11	17	mA
			Outputs Low		19	28	mA
			Outputs Disabled		20	31	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS374			DM74ALS374			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	30			35			MHz
T_{PLH}	Clock	Any Q		4		15	4		12	ns
T_{PHL}				4		15	4		12	ns
T_{PZH}	Output Control	Any Q		3		18	4		15	ns
T_{PZL}				4		21	5		18	ns
T_{PHZ}				2		12	2		10	ns
T_{PLZ}				2		15	3		13	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

Logic Diagram



Function Table

$\overline{\text{Output}}$ Control	Clock	D	Output Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of Q

Preliminary

National Semiconductor

DM54ALS/DM74ALS518,519,520,521,522
8-Bit Comparators

General Description

These comparators perform an "equal to" comparison of two eight-bit words with provision for expansion or external enabling. The matching of the two 8-bit input plus a logic LOW on the $\overline{EN}$ input produces the output A = B on the ALS518 & 519 and the output $\overline{A = B}$ on the ALS520, 521 & 522. The ALS520 & 521 have totem pole outputs, while the ALS518, 519 & 522 have open collector outputs for wire AND cascading. Additionally, the ALS518, 520 & 522 are provided with B input pull up termination resistors for analog or switch data.

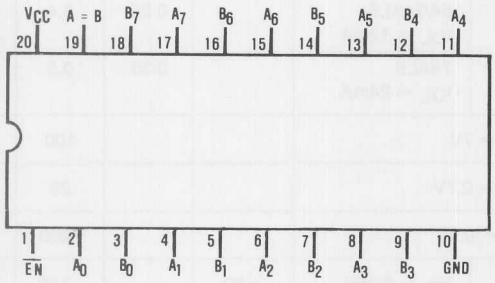
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with LS Family Counterpart.
- Improved Output Transient Handling Capability.

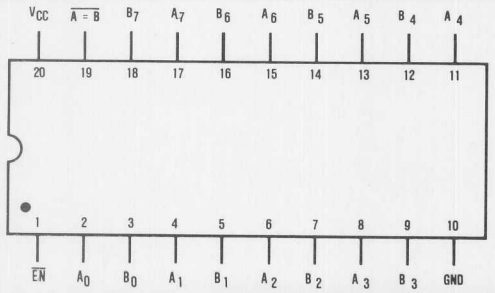
Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS518 (J) **74ALS518 (J,N)**
54ALS519 (J) **74ALS519 (J,N)**



54ALS520 (J) **74ALS520 (J,N)**
54ALS521 (J) **74ALS521 (J,N)**
54ALS522 (J) **74ALS522 (J,N)**

Function Tables

ALS518,519

Inputs		Output
$\overline{EN}$	Data	$\overline{A = B}$
L	A=B	H
L	A≠B	L
H	X	L

H = High Logic Level; L = Low Logic Level; X = Don't Care

ALS520,521,522

Inputs		Output
$\overline{EN}$	Data	$\overline{A = B}$
L	A=B	L
L	A≠B	H
H	X	H

H = High Logic Level; L = Low Logic Level; X = Don't Care

1

Recommended Operating Conditions

Parameter	DM54ALS 518,519,520,521,522			DM74ALS 518,519,520,521,522			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH} (ALS518,519,522)			5.5			5.5	V
High Level Output Current, I_{OH} (ALS520,521)			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −400μA	ALS520,521	V_{CC}−2			V
		I_{OH} = MAX		2.4	3.2		V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V	ALS518, 519,522			100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−200	μA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			10.5		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

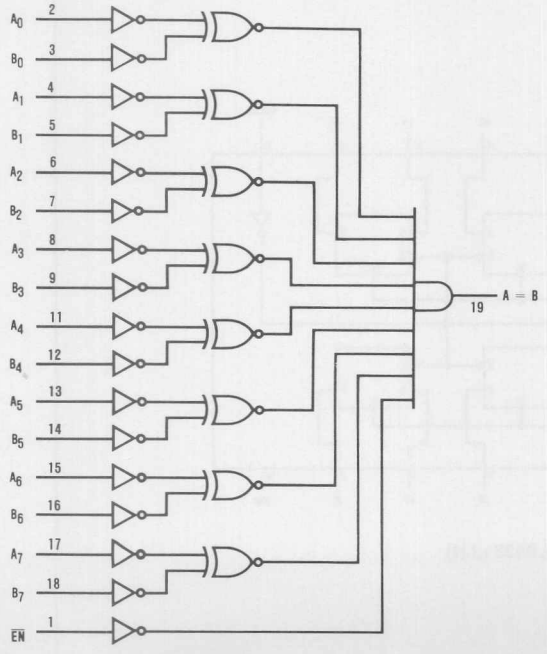
Parameter	From Input	To Output	Conditions	DM54ALS 518,519,522			DM74ALS 518,519,522			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation Delay Time, Low to high Level Output	A or B Data	$\overline{A=B}$ or $A=B$	V_{CC} = 4.5V to 5.5V, C_L = 50pF, R_L = 667Ω	5	15	35	5	15	26	ns
T_{PHL}, Propagation Delay Time, High to low Level Output				5	14	33	5	14	27	
T_{PLH}, Propagation Delay Time, Low to high Level Output	$\overline{EN}$			5	14	33	5	14	24	
T_{PHL}, Propagation Delay Time, High to low Level Output				4	12	28	4	12	23	

Switching Characteristics over recommended operating free air temperature range (Note 1)

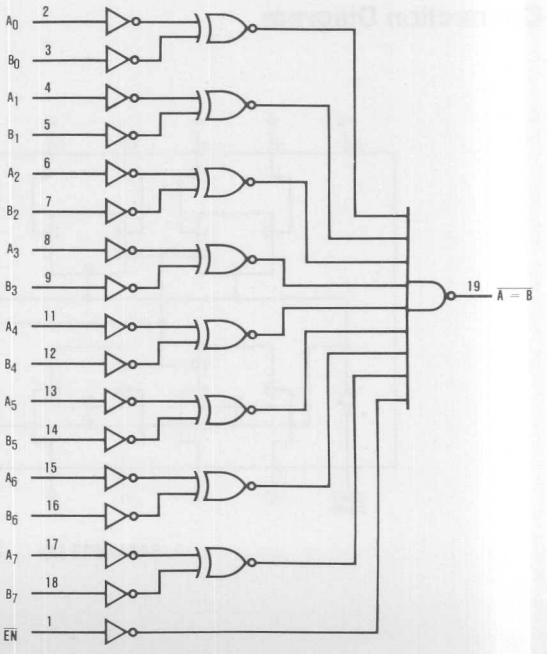
Parameter	From Input	To Output	Conditions	DM54ALS 520,521			DM74ALS 520,521			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation Delay Time, Low to high Level Output	A or B Data	$\overline{A=B}$	V_{CC} = 4.5V to 5.5V, C_L = 50pF, R_L = 500Ω	3	6.5	16	3	6.5	13	ns
T_{PHL}, Propagation Delay Time, High to low Level Output				4	8.5	22	4	8.5	17	
T_{PLH}, Propagation Delay Time, Low to high Level Output	$\overline{EN}$			3	5.5	14	3	5.5	11	
T_{PHL}, Propagation Delay Time, High to low Level Output				3	6.5	16	3	6.5	13	

NOTE 1: See notes pg. 1-iii, figures pg 3-4 and 3-1.

Logic Diagrams



54/74ALS518/519



54/74ALS520/521/522

National Semiconductor

Preliminary

DM54ALS533/DM74ALS533
Octal D-Type Transparent Latches With Inverted Outputs

General Description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the ALS533 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

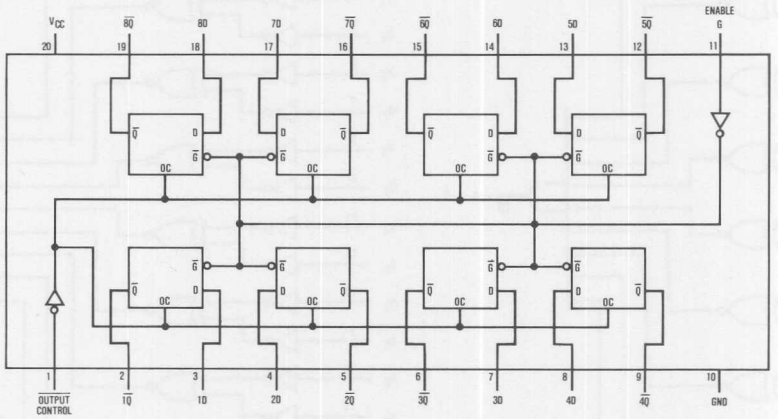
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced, Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS533	−55°C to 125°C
DM74ALS533	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS533 (J) **74ALS533 (J,N)**

Recommended Operating Conditions

Parameter	DM54ALS533			DM74ALS533			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA
Width of Enable Pulse, High or Low	15			15			ns
Data Setup Time, T_{SU}	10↓			10↓			ns
Data Hold Time, T_H	0↓			0↓			ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

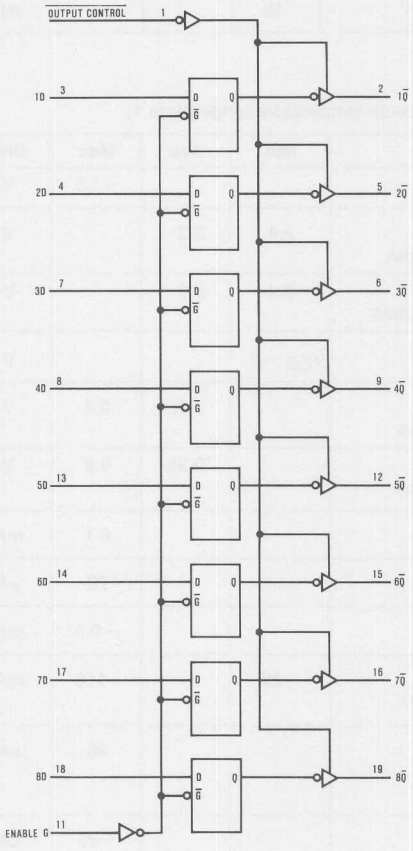
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} MAX	54/74ALS, I_{OH} = −1mA	2.4	3.2		V
			74ALS, I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS, I_{OL} = 12mA		0.25	0.4	V
			74ALS, I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS, V_O = 2.25V	−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V, V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, Outputs Open	Outputs High		10	15	mA
			Outputs Low		17	26	mA
			Outputs Disabled		18.5	28	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS533			DM74ALS533			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any $\overline{Q}$	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	3		15	3		12	ns
T_{PHL}				3		15	3		12	ns
T_{PLH}	Enable	Any $\overline{Q}$		8		25	8		20	ns
T_{PHL}				8		22	8		20	ns
T_{PZH}	Output Control	Any $\overline{Q}$		3		18	4		15	ns
T_{PZL}				4		21	5		18	ns
T_{PHZ}				2		12	2		10	ns
T_{PLZ}				3		15	3		13	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

Logic Diagram



Function Table

$\overline{\text{Output Control}}$	Enable G	D	Output $\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low state, H = High State, X = Don't Care
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

Preliminary

National Semiconductor

DM54ALS534/DM74ALS534 Octal D-Type Edge-Triggered Flip-Flops With Inverted Outputs

General Description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS534 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

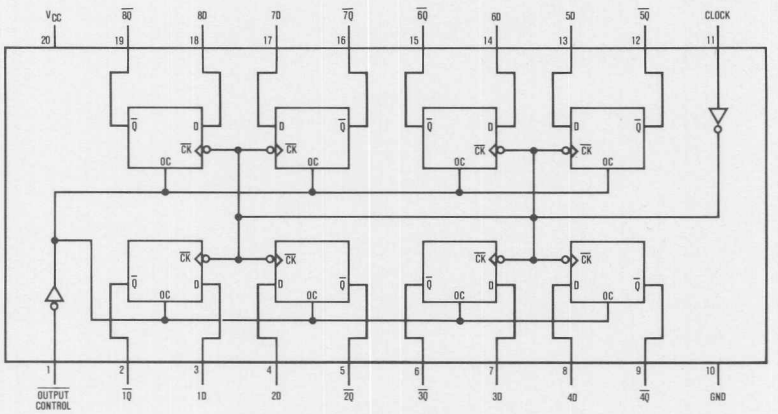
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS534	−55°C to 125°C
DM74ALS534	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS534 (J) 74ALS534 (J,N)

Recommended Operating Conditions

Parameter		DM54ALS534			DM74ALS534			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−1.0			−2.6	mA
Low Level Output Current, I_{OL}				12			24	mA
Clock frequency, f_{CLOCK}		0		30	0		35	MHz
Width of Clock Pulse, T_W	High	10			10			ns
	Low	17			15			ns
Data Setup Time, T_{SU}		10↑			10↑			ns
Data Hold Time, T_H		4↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

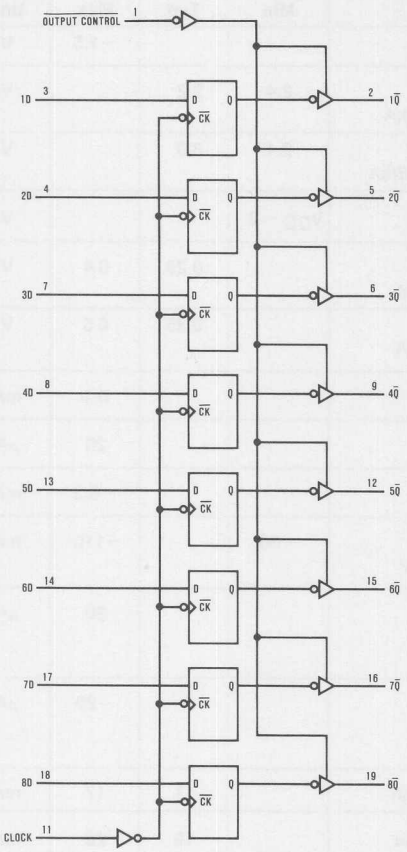
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		11	17	mA
			Outputs Low		19	28	mA
			Outputs Disabled		20	31	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS534			DM74ALS534			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	30			35			MHz
T_{PLH}	Clock	Any $\bar{Q}$		4		15	4		12	ns
T_{PHL}				4		15	4		12	ns
T_{PZH}	Output Control	Any $\bar{Q}$		3		18	4		15	ns
T_{PZL}				4		21	5		18	ns
T_{PHZ}				2		12	2		10	ns
T_{PLZ}				3		15	3		13	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

Logic Diagram



Function Table

Output Control	Clock	D	Output $\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor

Preliminary

DM54ALS/DM74ALS563,564 TRI-STATE® Inverting Octal D-Type Latches and Edge-Triggered Flip-Flops

Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

The ALS563 is identical to the ALS580. For detailed specification, refer to ALS580 data sheet.
The ALS564 is identical to the ALS576. For detailed specification, refer to ALS576 data sheet.

National Semiconductor

Preliminary

DM54ALS573/DM74ALS573 Octal D-Type Transparent Latches

General Description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ALS573 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

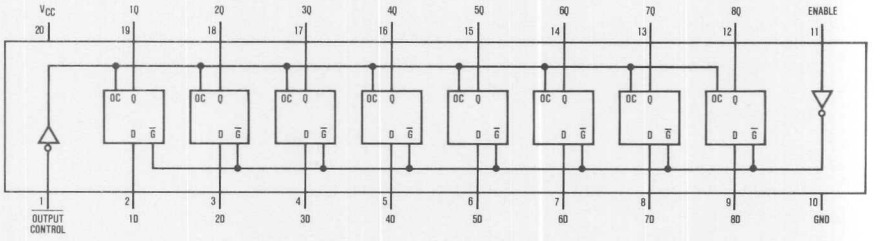
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally Equivalent with LS373.
- Improved AC Performance Over LS373 at Approximately Half the Power.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS573	−55°C to 125°C
DM74ALS573	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS573 (J) **74ALS573 (J,N)**

Recommended Operating Conditions

Parameter	DM54ALS573			DM74ALS573			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA
Width of Enable Pulse, High or Low	10			10			ns
Data Setup Time, T_{SU}	10↓			10↓			ns
Data Hold Time, T_H	7↓			7↓			ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V, V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, Outputs Open	Outputs High		10	14	mA
			Outputs Low		15	22	mA
			Outputs Disabled		15.5	24	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS573			DM74ALS573			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any Q	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	2		15	2		12	ns
T_{PHL}				2		15	2		12	ns
T_{PLH}	Enable	Any Q		8		27	8		20	ns
T_{PHL}				8		20	8		19	ns
T_{PZH}	Output Control	Any Q		4		21	4		18	ns
T_{PZL}				4		21	5		18	ns
T_{PHZ}				2		10	2		8	ns
T_{PLZ}				3		15	3		13	ns

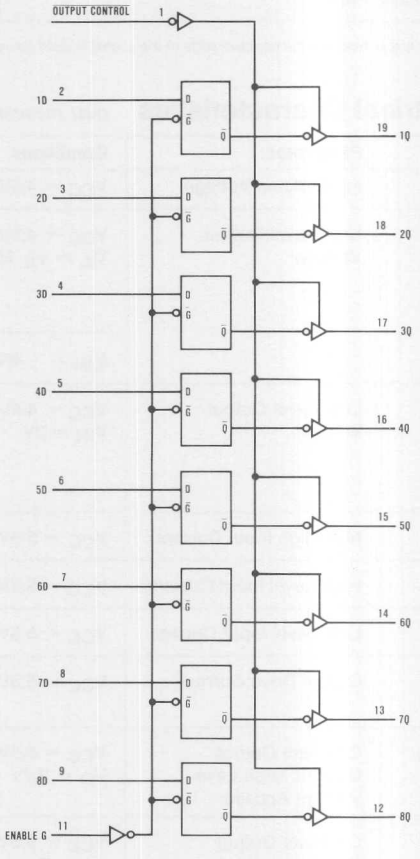
NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

Function Table

$\overline{\text{Output Control}}$	Enable G	D	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
Q_0 = Previous Condition of Q

Logic Diagram



National Semiconductor

Preliminary

DM54ALS574/DM74ALS574 Octal D-Type Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS574 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

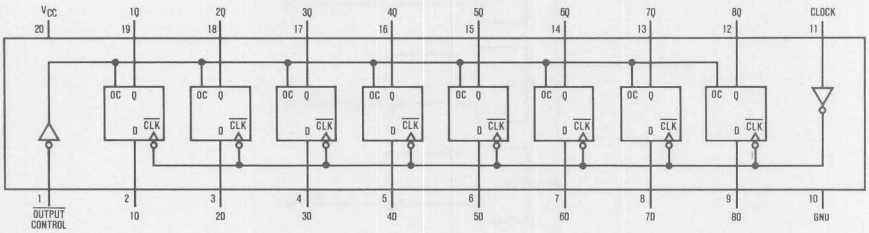
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally Equivalent with LS374.
- Improved AC Performance Over LS374 at Approximately Half the Power.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS574	−55°C to 125°C
DM74ALS574	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS574 (J) 74ALS574 (J,N)

Function Table

$\overline{\text{Output Control}}$	Clock	D	Output Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

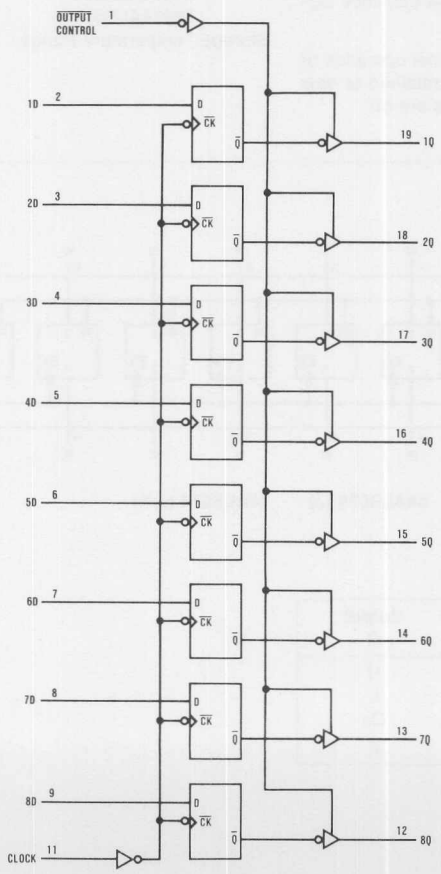
L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of Q

Recommended Operating Conditions

Parameter		DM54ALS574			DM74ALS574			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−1.0			−2.6	mA
Low Level Output Current, I_{OL}				12			24	mA
Clock frequency, f_{CLOCK}		0		30	0		35	MHz
Width of Clock Pulse, T_W	High	10			10			ns
	Low	17			15			ns
Data Setup Time, T_{SU}		10↑			10↑			ns
Data Hold Time, T_H		4↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Logic Diagram



Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		10.5	17	mA
			Outputs Low		14.5	23	mA
			Outputs Disabled		15.5	27	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS574			DM74ALS574			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	30			35			MHz
T_{PLH}	Clock	Any Q		4		15	4		12	ns
T_{PHL}				4		15	4		12	ns
T_{PZH}	Output Control	Any Q		4		21	5		18	ns
T_{PZL}				4		21	5		18	ns
T_{PHZ}	Output Control	Any Q		2		10	2		8	ns
T_{PLZ}				3		15	3		13	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

National Semiconductor

Preliminary

DM54ALS576/DM74ALS576 Octal D-Type Edge-Triggered Flip-Flops With Inverted Outputs

General Description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS576 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

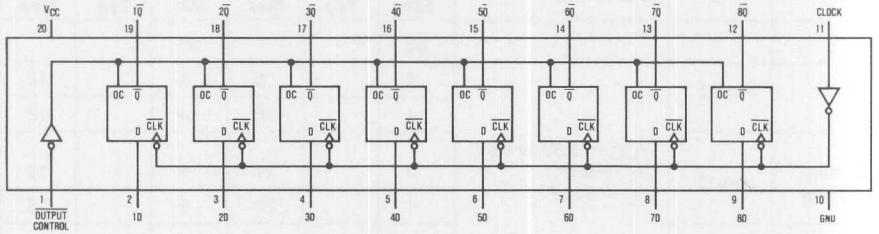
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS576	−55°C to 125°C
DM74ALS576	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS576 (J) **74ALS576 (J,N)**

Recommended Operating Conditions

Parameter		DM54ALS576			DM74ALS576			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−1.0			−2.6	mA
Low Level Output Current, I_{OL}				12			24	mA
Clock frequency, f_{CLOCK}		0		30	0		35	MHz
Width of Clock Pulse, T_W	High	10			10			ns
	Low	17			15			ns
Data Setup Time, T_{SU}		10↑			10↑			ns
Data Hold Time, T_H		4↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		10.5	17	mA
			Outputs Low		14.5	23	mA
			Outputs Disabled		15.5	27	mA

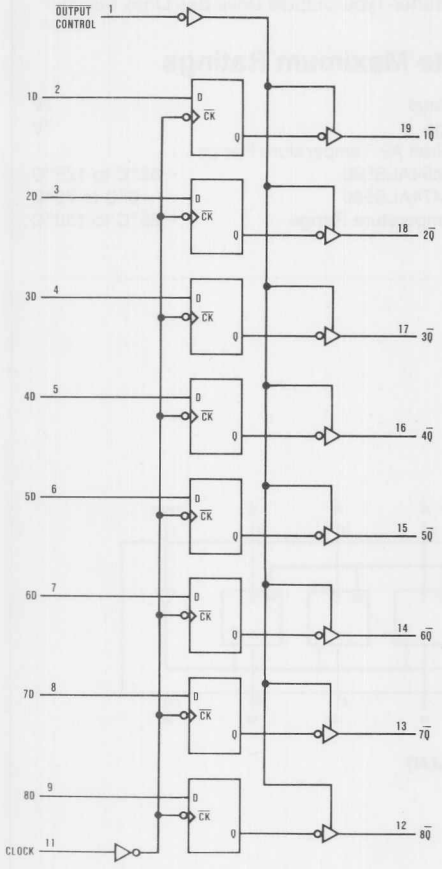
Switching Characteristics

over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS576			DM74ALS576			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	30			35			MHz
T_{PLH}	Clock	Any $\overline{Q}$		4		15	4		12	ns
T_{PHL}				4		15	4		12	ns
T_{PZH}	Output Control	Any $\overline{Q}$		4		21	4		18	ns
T_{PZL}				4		21	4		18	ns
T_{PHZ}				2		10	2		8	ns
T_{PLZ}				3		15	3		13	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

Logic Diagram



Function Table

$\overline{\text{Output}}$ Control	Clock	D	Output $\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

1

National Semiconductor

Preliminary

DM54ALS580/DM74ALS580 Octal D-Type Transparent Latches With Inverted Outputs

General Description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the ALS580 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

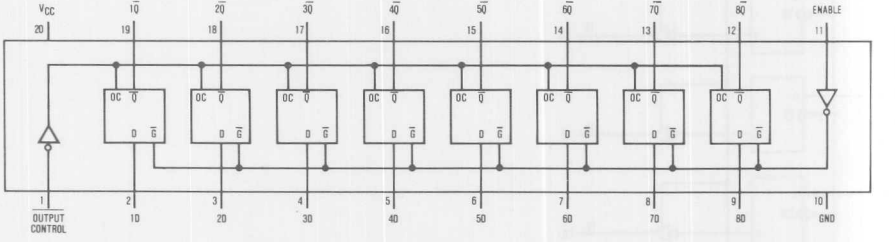
Features

- Switching Specifications at 50pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced, Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS580	−55°C to 125°C
DM74ALS580	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS580 (J) 74ALS580 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS580			DM74ALS580			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA
Width of Enable Pulse, High or Low	15			15			ns
Data Setup Time, T_{SU}	10↓			10↓			ns
Data Hold Time, T_H	0↓			0↓			ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

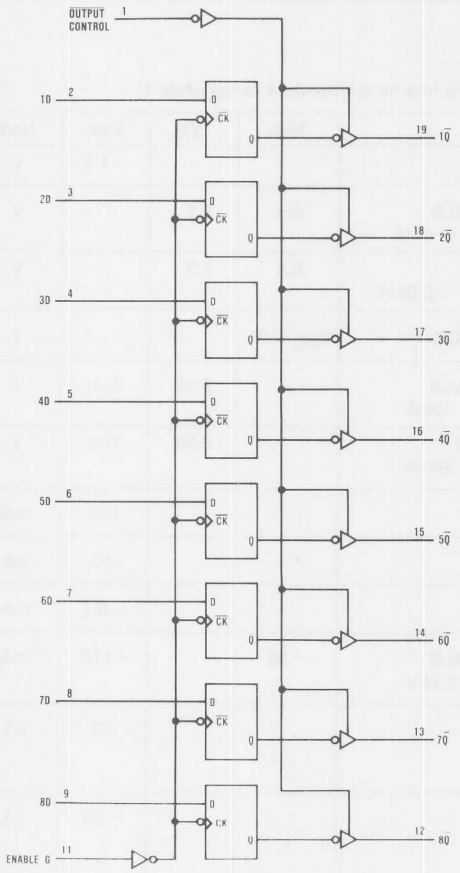
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		10	16	mA
			Outputs Low		15	24	mA
			Outputs Disabled		15.5	26	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS580			DM74ALS580			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any $\overline{Q}$	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	3		21	3		18	ns
T_{PHL}				3		15	3		12	ns
T_{PLH}	Enable	Any $\overline{Q}$		8		27	8		22	ns
T_{PHL}				8		22	8		21	ns
T_{PZH}	Output Control	Any $\overline{Q}$		4		21	4		18	ns
T_{PZL}				4		21	4		18	ns
T_{PHZ}				2		10	2		8	ns
T_{PLZ}				3		15	3		13	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

Logic Diagram



Function Table

Output Control	Enable G	D	Output $\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor

Preliminary

DM54ALS/DM74ALS689 8-Bit Comparator

General Description

This comparator performs an "equal to" comparison of two eight-bit words with provision for expansion or external enabling. The matching of the two 8-bit input plus a logic LOW on the $\overline{EN}$ input produces the output $\overline{A = B}$. The ALS 689 has an open collector output for wire AND cascading.

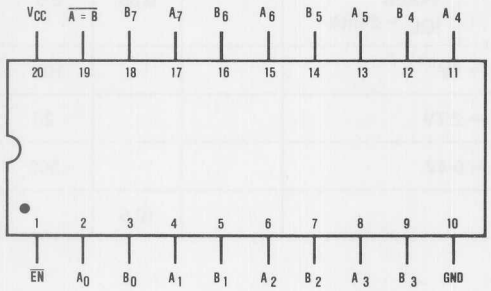
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with LS Family TTL Counterpart.
- Improved Output Transient Handling Capability.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS689	−55°C to 125°C
DM74ALS689	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS689 (J) 74ALS689 (J,N)

Function Table

Inputs		Output
$\overline{EN}$	Data	$\overline{A=B}$
L	A=B	L
L	A≠B	H
H	X	H

H = High Level, L = Low Level, X = Don't Care

Recommended Operating Conditions

Parameter	DM54ALS689			DM74ALS689			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

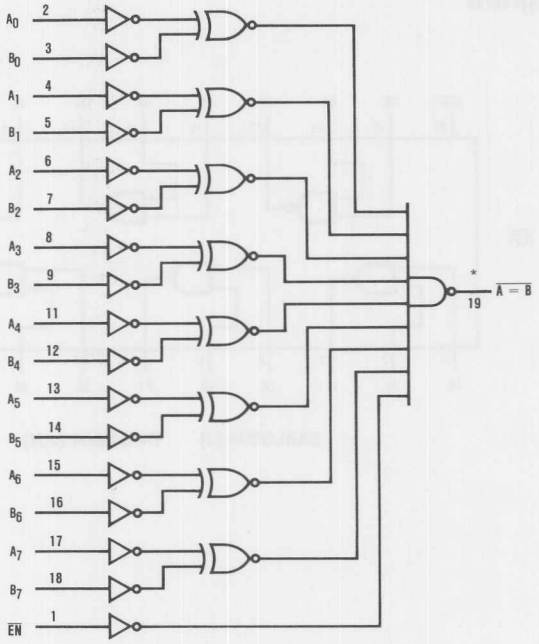
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−200	μA
I_{CC}	Supply Current	V_{CC} = 5.5V			10.5		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From Input	To Output	Conditions	DM54ALS689			DM74ALS689			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation Delay Time, Low to high Level Output	A or B Data	$\overline{A=B}$	V_{CC}: 4.5V to 5.5V C_L = 50pF R_L = 667Ω	3	13	31	3	13	23	ns
T_{PHL}, Propagation Delay Time, High to low Level Output				4	12	30	4	12	24	
T_{PLH}, Propagation Delay Time, Low to high Level Output	$\overline{EN}$			3	12	29	3	12	21	
T_{PHL}, Propagation Delay Time, High to low Level Output				3	10	24	3	10	20	

NOTE 1: See notes pg. 1-iii, figures pg 3-4.

Logic Diagram



* Output is open collector

National Semiconductor

Preliminary

DM54ALS804/DM74ALS804 Hex 2-Input NAND Drivers

Features

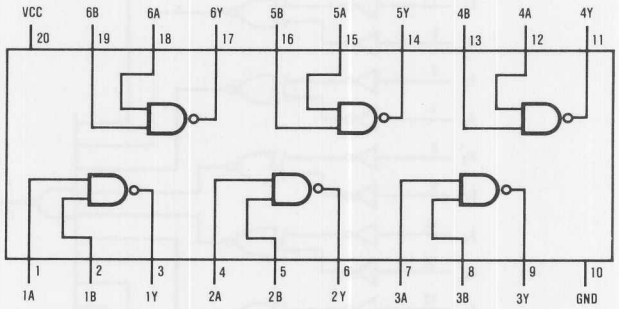
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{AB}$



54ALS804 (J) **74ALS804 (J,N)**

Recommended Operating Conditions

Parameter	DM54ALS804			DM74ALS804			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
		I_{OH} = MAX		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74 ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.14		mA
			Outputs Low		1.2		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS804			DM74ALS804			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1.4	2.9	7.0	1.4	2.9	6.0	ns
T_{PHL}, Propagation delay time. High to low level output		1.2	2.5	6.0	1.2	2.5	5.0	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS805/DM74ALS805 Hex 2-Input NOR Drivers

Features

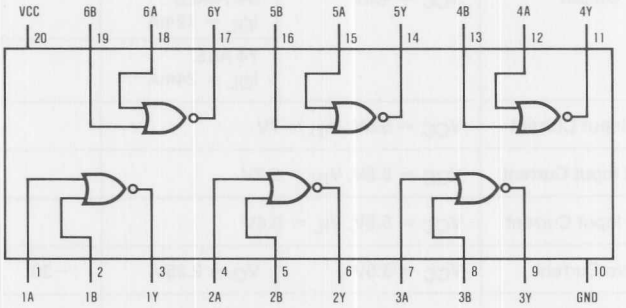
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{A+B}$



54ALS805 (J) 74ALS805 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS805			DM74ALS805			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
		I_{OH} = MAX		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74 ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.28		mA
			Outputs Low		1.4		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS805			DM74ALS805			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1.7	3.4	8.5	1.7	3.4	7.0	ns
T_{PHL}, Propagation delay time. High to low Level Output		1.2	2.5	6.5	1.2	2.5	5.0	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS808/DM74ALS808 Hex 2-Input AND Drivers

Features

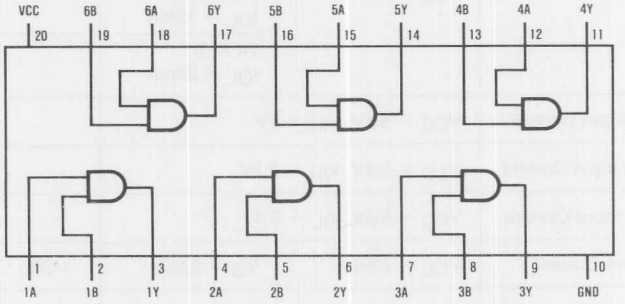
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{AB}$



54ALS808 (J) **74ALS808 (J,N)**

Recommended Operating Conditions

Parameter	DM54ALS808			DM74ALS808			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −.4mA		V_{CC}−2			V
		I_{OH} = MAX		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74 ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.53		mA
			Outputs Low		1.3		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS808			DM74ALS808			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	2.0	3.9	10.0	2.0	3.9	8.0	ns
T_{PHL}, Propagation delay time. High to low Level Output		2.3	4.6	11.5	2.3	4.6	9.5	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS832/DM74ALS832 Hex 2-Input OR Drivers

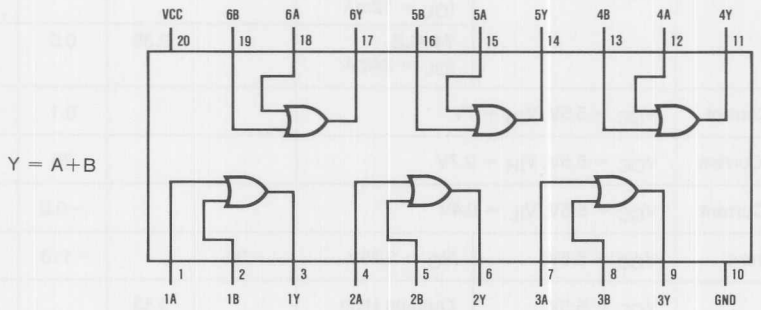
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



Y = A+B

54ALS832 (J) 74ALS832 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS832			DM74ALS832			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −.4mA		V_{CC}−2			V
		I_{OH} = MAX		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74 ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.7		mA
			Outputs Low		1.4		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS832			DM74ALS832			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	2.0	3.9	10.0	2.0	3.9	8.0	ns
T_{PHL}, Propagation delay time. High to low Level Output		2.5	5.1	9.0	2.5	5.1	10.5	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

DM54ALS873/DM74ALS873
Dual 4-Bit D-Type Transparent Latches

General Description

These Dual 4-Bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ALS873 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output conrol does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

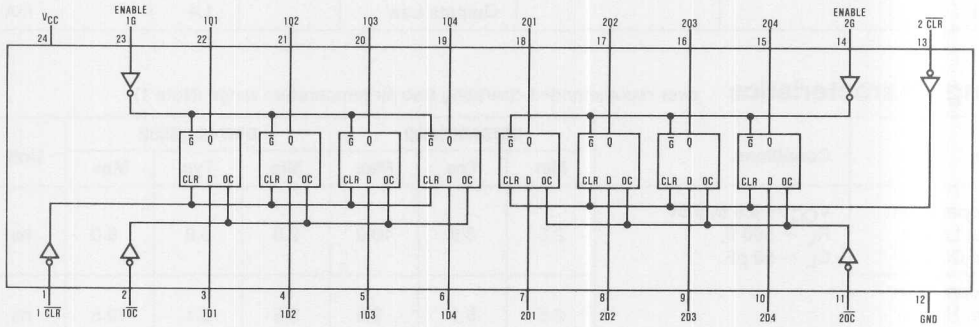
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS873	−55°C to 125°C
DM74ALS873	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS873 (J) **74ALS873 (J,N)**

Recommended Operating Conditions

Parameter	DM54ALS873			DM74ALS873			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA
Pulse Width, T_W Enable High Clear Low	10 15			10 15			ns
Data Setup Time, T_{SU}	10↓			10↓			ns
Data Hold Time, T_H	7↓			7↓			ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		10	21	mA
			Outputs Low		15	29	mA
			Outputs Disabled		15.5	31	mA

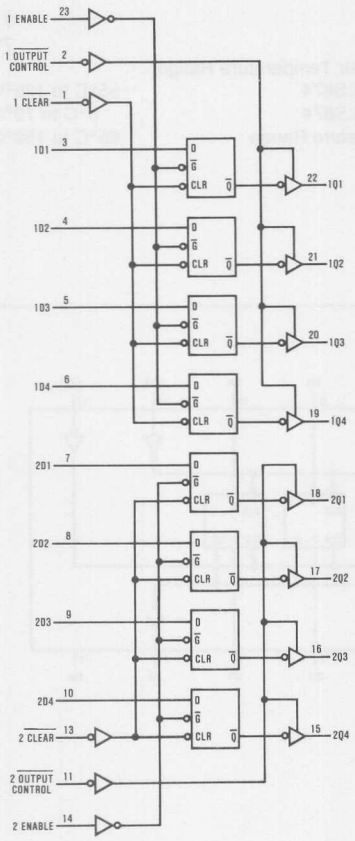
Switching Characteristics

over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS873			DM74ALS873			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any Q	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	2		15	2		12	ns
T_{PHL}				2		15	2		12	ns
T_{PLH}	Enable	Any Q		8		29	8		21	ns
T_{PHL}				8		22	8		21	ns
T_{PZH}	Output Control	Any Q		4		21	4		18	ns
T_{PZL}				4		21	4		18	ns
T_{PHZ}				2		10	2		8	ns
T_{PLZ}				2		15	2		13	ns
T_{PHL}	Clear	Any Q		6		24	6		24	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

Logic Diagram



Function Table

$\overline{CLR}$	D	EN	$\overline{OC}$	Q
X	X	X	H	Z
L	X	X	L	L
H	H	H	L	H
H	L	H	L	L
H	X	L	L	Q_0

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
Q_0 = Previous Condition of Q

National Semiconductor

DM54ALS874/DM74ALS874
Dual 4-Bit D-Type Edge-Triggered Flip-Flops

General Description

These Dual 4-Bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS874 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

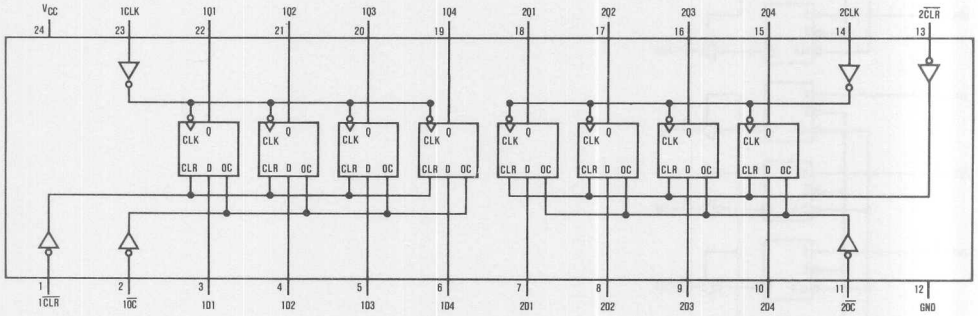
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS874	−55°C to 125°C
DM74ALS874	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS874 (J) **74ALS874 (J,N)**

Recommended Operating Conditions

Parameter		DM54ALS874			DM74ALS874			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−1.0			−2.6	mA
Low Level Output Current, I_{OL}				12			24	mA
Clock frequency, f_{CLOCK}		0		30	0		35	MHz
Width of Clock Pulse, T_W	High	10			10			ns
	Low	17			15			ns
Width of Clear Pulse, T_W	Low	10			10			ns
Data Setup Time, T_{SU}		10↑			10↑			ns
Data Hold Time, T_H		4↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		14	21	mA
			Outputs Low		18	29	mA
			Outputs Disabled		20	31	mA

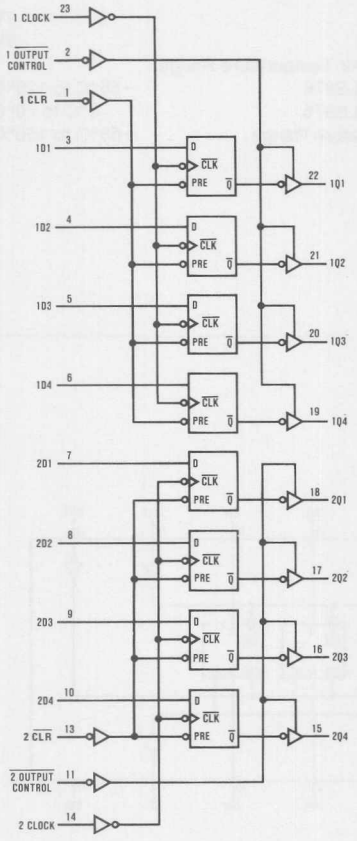
Switching Characteristics

over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS874			DM74ALS874			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	30			35			MHz
T_{PLH}	Clock	Any Q		4		15	4		12	ns
T_{PHL}				4		15	4		12	ns
T_{PZH}	Output Control	Any Q		4		21	4		18	ns
T_{PZL}				4		21	4		18	ns
T_{PHZ}				2		10	2		8	ns
T_{PLZ}				3		15	3		13	ns
T_{PHL}	Clear	Any Q		6		22	6		19	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

Logic Diagram



Function Table

$\overline{CLR}$	D	CLK	$\overline{OC}$	Q
X	X	X	H	Z
L	X	X	L	L
H	H	↑	L	H
H	L	↑	L	L
H	X	L	L	Q_0

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of Q

National Semiconductor

DM54ALS876/DM74ALS876 Dual 4-Bit D-Type Edge-Triggered Flip-Flops With Inverted Outputs

General Description

These inverting Dual 4-Bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS876 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

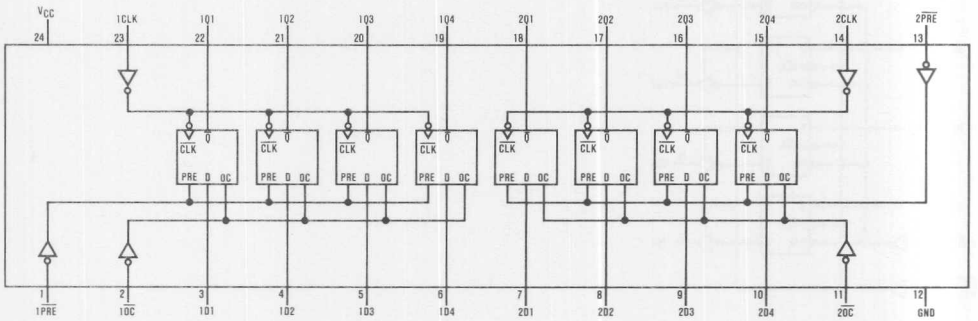
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS876	−55°C to 125°C
DM74ALS876	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS876 (J) 74ALS876 (J,N)

Recommended Operating Conditions

Parameter		DM54ALS876			DM74ALS876			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−1.0			−2.6	mA
Low Level Output Current, I_{OL}				12			24	mA
Clock frequency, f_{CLOCK}		0		30	0		35	MHz
Width of Clock Pulse, T_W	High	10			10			ns
	Low	17			15			ns
Width of Preset Pulse, T_W	Low	10			10			ns
Data Setup Time, T_{SU}		10↑			10↑			ns
Data Hold Time, T_H		4↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		14	21	mA
			Outputs Low		18	29	mA
			Outputs Disabled		20	31	mA

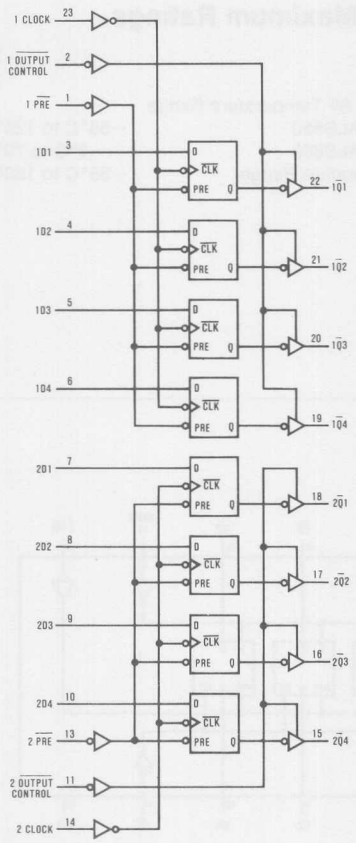
Switching Characteristics

over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS876			DM74ALS876			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	30			35			MHz
T_{PLH}	Clock	Any $\overline{Q}$		4		15	4		12	ns
T_{PHL}				4		15	4		12	ns
T_{PZH}	Output Control	Any $\overline{Q}$		4		21	4		18	ns
T_{PZL}				4		21	4		18	ns
T_{PHZ}				2		10	2		8	ns
T_{PLZ}				3		15	3		13	ns
T_{PHL}	Preset	Any $\overline{Q}$		6		22	6		19	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

Logic Diagram



Function Table

$\overline{PRE}$	D	CLK	$\overline{OC}$	$\overline{Q}$
X	X	X	H	Z
L	X	X	L	L
H	H	↑	L	L
H	L	↑	L	H
H	X	L	L	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor

DM54ALS880/DM74ALS880 Dual 4-Bit D-Type Transparent Latches With Inverted Outputs

General Description

These Dual 4-Bit inverting registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the ALS880 are transparent D-type latches meaning that while the enable (G) is high the $\overline{Q}$ outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

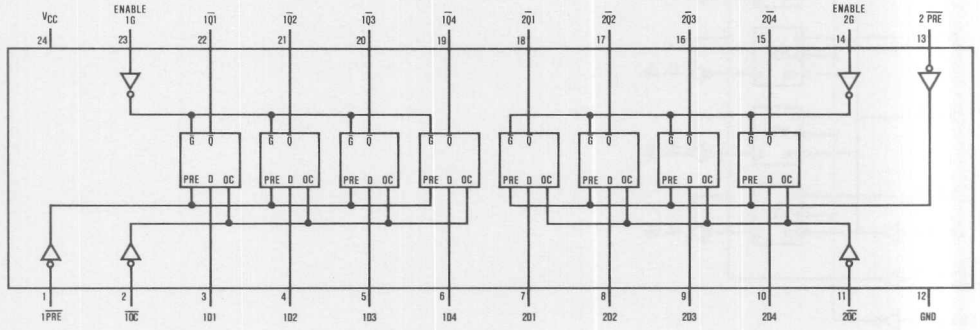
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS880	−55°C to 125°C
DM74ALS880	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS880 (J) 74ALS880 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS880			DM74ALS880			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA
Pulse Width, T_W Enable Preset Low	15 15			15 15			ns ns
Data Setup Time, T_{SU}	18↓			15↓			ns
Data Hold Time, T_H	0↓			0↓			ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		14	21	mA
			Outputs Low		19	29	mA
			Outputs Disabled		20	31	mA

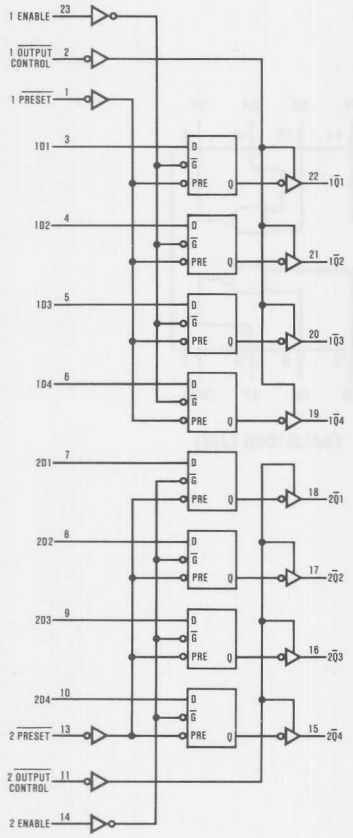
Switching Characteristics

over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54ALS880			DM74ALS880			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any $\overline{Q}$	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	3		23	3		20	ns
T_{PHL}				3		15	3		12	ns
T_{PLH}	Enable	Any $\overline{Q}$		8		31	8		24	ns
T_{PHL}				8		22	8		21	ns
T_{PZH}	Output Control	Any $\overline{Q}$		4		21	5		18	ns
T_{PZL}				4		21	5		18	ns
T_{PHZ}				2		10	2		8	ns
T_{PLZ}				3		15	3		13	ns
T_{PHL}	Preset	Any $\overline{Q}$		6		24	6		21	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

Logic Diagram



Function Table

$\overline{PRE}$	D	EN	$\overline{OC}$	$\overline{Q}$
X	X	X	H	Z
L	X	X	L	L
H	H	H	L	L
H	L	H	L	H
H	X	L	L	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

1

National Semiconductor

Preliminary

DM54ALS1000/DM74ALS1000
Quadruple 2-Input NAND Buffers

Features

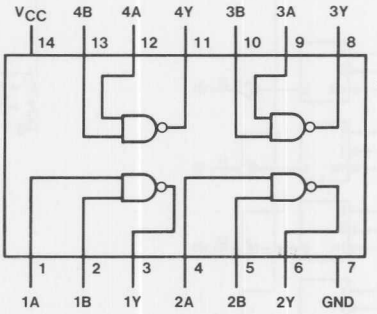
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS1000	−55°C to 125°C
DM74ALS1000	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{AB}$



54ALS1000 (J) 74ALS1000 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS1000			DM74ALS1000			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			0.86	1.6	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			4.0	6.4	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS1000			DM74ALS1000			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	2		10	2		8	ns
T_{PHL}, Propagation delay time. High to low Level Output		3		10	3		8	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS1002/DM74ALS1002
Quadruple 2-Input Positive-Nor Buffers

Features

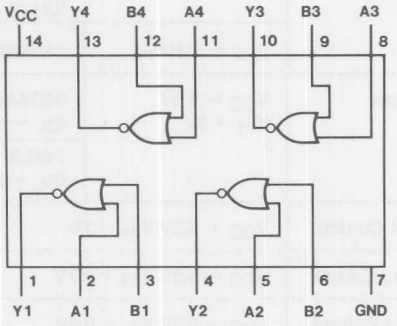
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS1002	−55°C to 125°C
DM74ALS1002	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$$Y = \overline{A + B}$$



54ALS1002 (J) 74ALS1002 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS1002			DM74ALS1002			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			1.7	2.8	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			4.8	8.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS1002			DM74ALS1002			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	2		10	2		8	ns
T_{PHL}, Propagation delay time. High to low Level Output		3		10	3		8	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS1003/DM74ALS1003 Quadruple 2-Input NAND Buffers with Open-Collector Outputs

Features

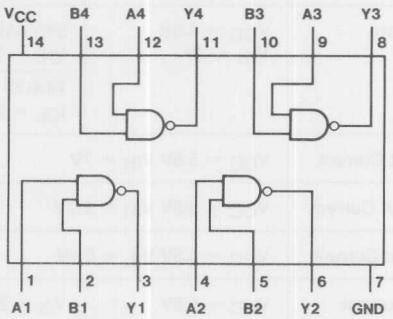
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved Line Receiving Characteristics.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Off State (High Level) Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS1003	−55°C to 125°C
DM74ALS1003	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{AB}$



54ALS1003 (J) 74ALS1003 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS1003			DM74ALS1003			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			0.86	1.6	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			4.0	6.4	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS1003			DM74ALS1003			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 667 Ω, C_L = 50 pF.	10		40	10		30	ns
T_{PHL}, Propagation delay time. High to low Level Output		7		18	7		15	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-4.

National Semiconductor

Preliminary

DM54ALS1004/DM74ALS1004 Hex Inverting Drivers

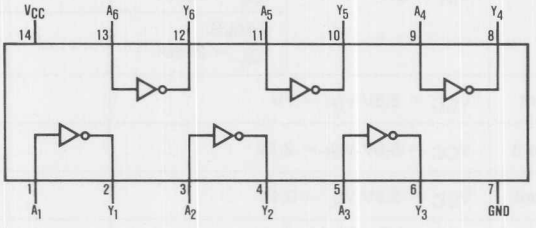
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS1004 (J) 74ALS1004 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS1004			DM74ALS1004			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
		I_{OH} = MAX		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74 ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.14		mA
			Outputs Low		1.2		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS1004			DM74ALS1004			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1.4	2.8	7.5	1.4	2.8	6.0	ns
T_{PHL}, Propagation delay time. High to low Level Output		1.2	2.4	6.5	1.2	2.4	5.0	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS1005/DM74ALS1005 Hex Inverting Drivers with Open Collector Outputs

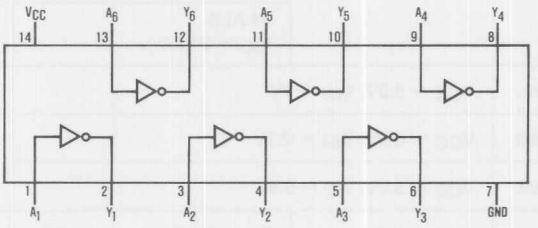
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS1005 (J) 74ALS1005 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS1005			DM74ALS1005			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74 ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.14		mA
			Outputs Low		1.2		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS1005			DM74ALS1005			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V, R_L = 667 Ω, C_L = 50 pF.	7	10	25	7	10	20	ns
T_{PHL}, Propagation delay time. High to low Level Output		1.2	3	6.5	1.2	3	5	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-4.

National Semiconductor

Preliminary

DM54ALS1008/DM74ALS1008 Quadruple 2-Input AND Buffers

Features

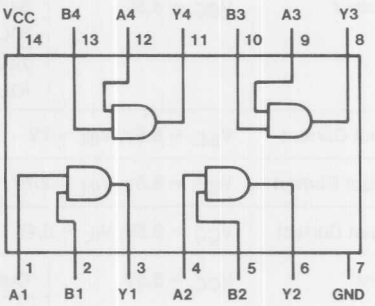
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS1008	−55°C to 125°C
DM74ALS1008	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = AB$



54ALS1008 (J) 74ALS1008 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS1008			DM74ALS1008			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IL} = .8V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 4.5V			1.7	2.8	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 0V			4.8	8.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS1008			DM74ALS1008			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	3		12	3		10	ns
T_{PHL}, Propagation delay time. High to low Level Output		4		12	4		10	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS1010/DM74ALS1010
Triple 3-Input NAND Buffers

Features

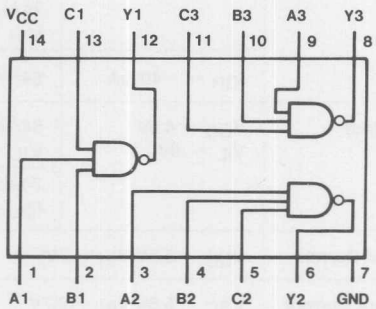
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS1010	−55°C to 125°C
DM74ALS1010	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{ABC}$



54ALS1010 (J) 74ALS1010 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS1010			DM74ALS1010			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			0.65	1.1	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			3.1	5.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS1010			DM74ALS1010			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	2		11	2		9	ns
T_{PHL}, Propagation delay time. High to low Level Output		3		11	3		9	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS1011/DM74ALS1011
Triple 3-Input AND Buffers

Features

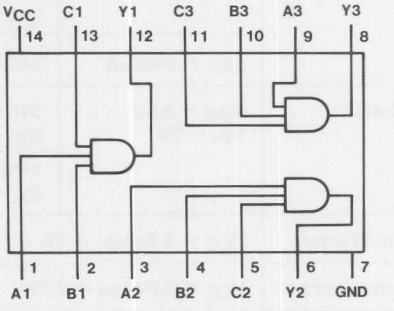
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS1011	−55°C to 125°C
DM74ALS1011	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = ABC$



54ALS1011 (J) 74ALS1011 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS1011			DM74ALS1011			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IL} = .8V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 4.5V			1.2	2.0	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 0V			3.6	5.8	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS1011			DM74ALS1011			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	3		13	3		11	ns
T_{PHL}, Propagation delay time. High to low Level Output		4		13	4		11	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS1020/DM74ALS1020
Dual 4-Input NAND Buffers

Features

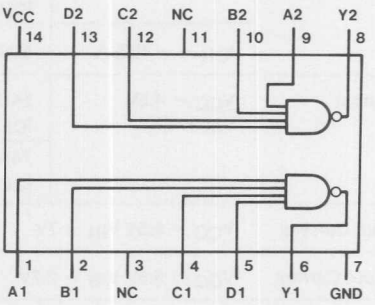
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS1020	−55°C to 125°C
DM74ALS1020	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$$Y = \overline{ABCD}$$



54ALS1020 (J) 74ALS1020 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS1020			DM74ALS1020			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 0V			0.43	0.8	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 4.5V			2.0	3.2	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS1020			DM74ALS1020			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	2		10	2		8	ns
T_{PHL}, Propagation delay time. High to low Level Output		3		10	3		8	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS1032/DM74ALS1032 Quadruple 2-Input OR Buffers

Features

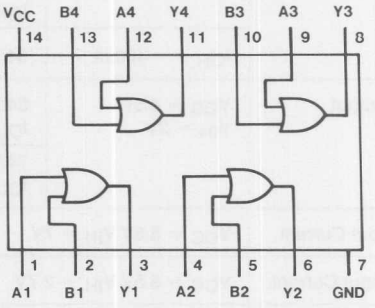
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS1032	−55°C to 125°C
DM74ALS1032	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = A + B$



54ALS1032 (J) 74ALS1032 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS1032			DM74ALS1032			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OH} = −1mA	2.4	3.2		V
			74ALS I_{OH} = −2.6mA	2.4	3.3		V
		I_{OH} = −400μA	54/74ALS	V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = .8V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CCH}	Supply Current	Outputs High V_{CC} = 5.5V, VI = 4.5V			2.3	4.0	mA
I_{CCL}	Supply Current	Outputs Low V_{CC} = 5.5V, VI = 0V			5.6	9.1	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS1032			DM74ALS1032			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF.	3		12	3		10	ns
T_{PHL}, Propagation delay time. High to low Level Output		4		12	4		10	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS1034/DM74ALS1034 Hex Non-Inverting Drivers

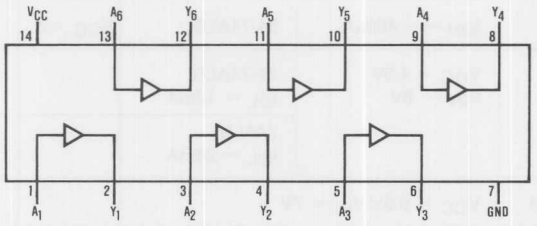
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS1034 (J) 74ALS1034 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS1034			DM74ALS1034			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
		I_{OH} = MAX		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74 ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.53		mA
			Outputs Low		1.3		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS1034			DM74ALS1034			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1.8	4.0	10	2.2	4.5	9	ns
T_{PHL}, Propagation delay time. High to low Level Output		2.2	4.5	12	2.2	4.5	9	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

DM54ALS1035/DM74ALS1035 Hex Non-Inverting Drivers with Open Collector Outputs

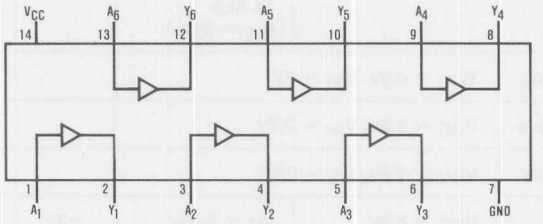
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54ALS1035 (J) 74ALS1035 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS1035			DM74ALS1035			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12mA		0.25	0.4	V
			74 ALS I_{OL} = 24mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.53		mA
			Outputs Low		1.3		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS1035			DM74ALS1035			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 667 Ω, C_L = 50 pF.	7	12	30	7	12	25	ns
T_{PHL}, Propagation delay time. High to low Level Output		2	4.5	12	2	4.5	9	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-4.

National Semiconductor

Preliminary

DM54ALS/DM74ALS1240, 1241, 1242, 1243, 1244 TRI-STATE® Bus Drivers/Receivers

General Description

This family of Advance Low Power Schottky TRI-STATE Bus circuits are designed to provide either bidirectional or unidirectional buffer interface in Memory, Microprocessor, and Communication Systems. The output characteristics of the circuits have low impedance sufficient to drive terminated transmission lines. The input characteristics of the circuits likewise have a high impedance so it will not significantly load the transmission line. The package contains eight TRI-STATE buffers organized with four buffers having a common TRI-STATE enable gate. The ALS1240, 1241 and 1244 are eight wide in a 20 pin package, and may be used as a 4 wide bidirectional or eight wide unidirectional. The ALS1242 and 1243 are organized four wide bidirectional in a 14 pin package. The buffer selection includes inverting and non-inverting, with enable or disable TRI-STATE control. The TRI-STATE circuitry contains a feature that maintains the buffers in TRI-STATE until the power supply (V_{CC}) is greater than 3V. This feature prevents the buffers from glitching the system bus during power up or down.

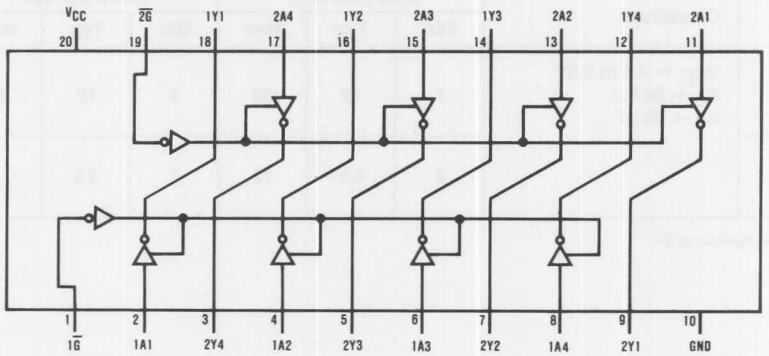
Features

- Lower Power Version of 54ALS240/241/242/243/244
- Advanced Low Power Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Switching Performance with Less Power Dissipation Compared with 54/74LS Counterpart.
- Functional and Pin Compatible with 54/74LS Counterpart.
- Switching Response Specified Into 500 ohm and 50 pF.
- Low Level Drive Current
  74ALS-1 24ma , 74ALS 16ma , 54ALS 8ma
- Glitch Free Bus During Power Up/Down.
- Specified To Interface With CMOS
  At VOH = V_{CC} − 2V.

Absolute Maximum Ratings

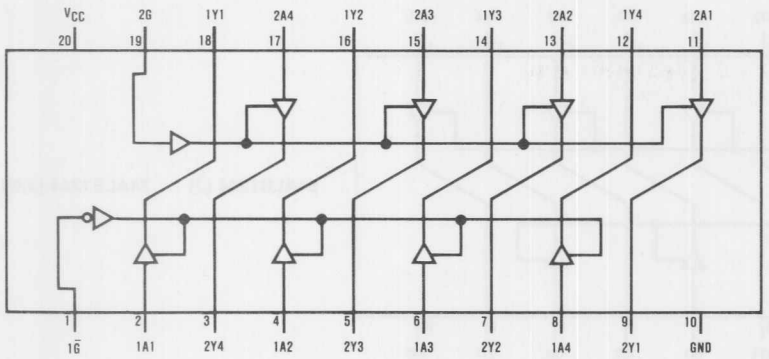
Supply Voltage, V_{CC}	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54ALS	−55°C to 125°C
DM74ALS	0°C to 70.C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
(Soldering, 10 seconds)	+300°C

Connection Diagram

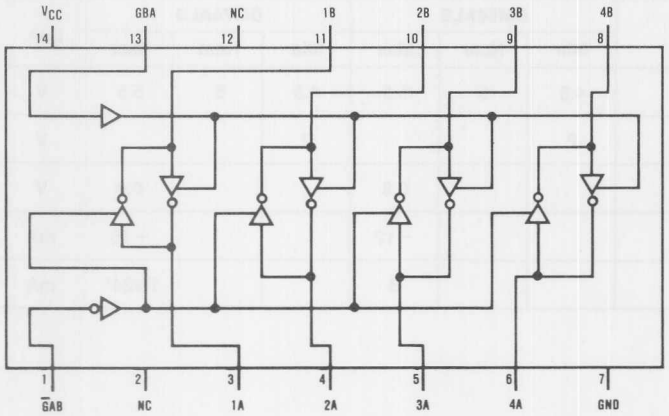


54ALS1240 (J) 74ALS1240 (J,N)

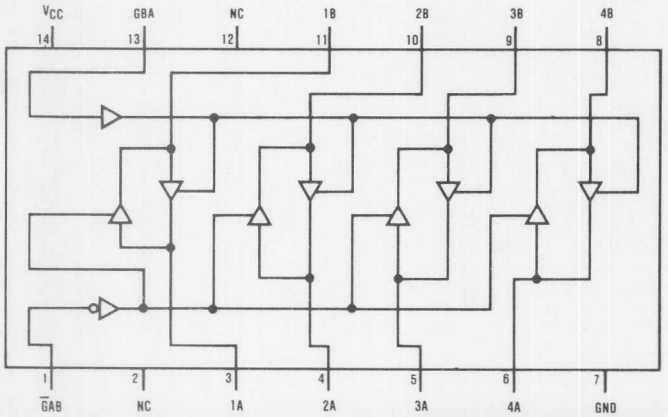
Connection Diagrams



54ALS1241 (J) **74ALS1241 (J,N)**

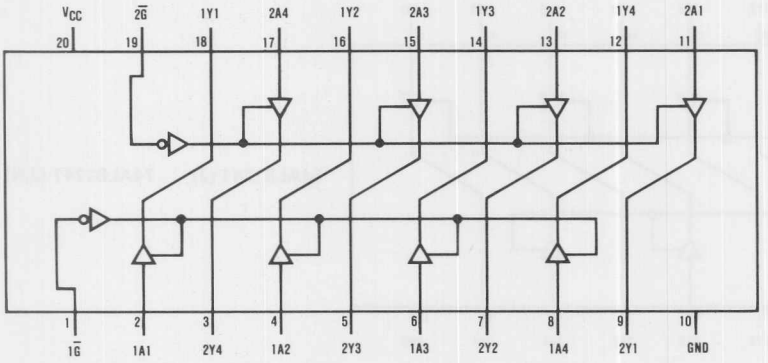


54ALS1242 (J) **74ALS1242 (J,N)**



54ALS1243 (J) **74ALS1243 (J,N)**

Connection Diagrams



54ALS1244 (J) 74ALS1244 (J,N)

Recommended Operating Conditions

Parameter	DM54ALS			DM74ALS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			8			16/24*	mA

* Applies to 74ALS-1 options.

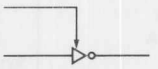
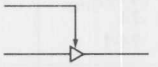
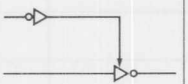
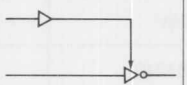
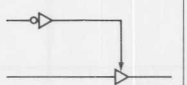
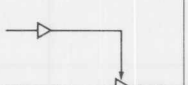
Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions	Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = −3mA V_{CC} = 4.5V, I_{OH} = −15mA I_{OH} = −400μA	2.4 2.0 V_{CC}−2	3.2 2.3		V V V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = 8mA 54/74 I_{OL} = 16mA 74 I_{OL} = 24mA 74-1		.25 .35 .35	.40 .50 .50	V V V
I_{IX}	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V			100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V			−200	μA
I_{OZH}	High Level TRI-STATE® Output Current	V_{CC} = 5.5V, V = 2.7V			20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V = .4V			−20	μA
I_{OD}	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V 54/74ALS1240 Outputs High Outputs Low TRI-STATE				mA
I_{CC}	Supply Current	V_{CC} = 5.5V 54/74ALS1241 Outputs High Outputs Low TRI-STATE				mA
I_{CC}	Supply Current	V_{CC} = 5.5V 54/74ALS1242 A Port Outputs High A Port Outputs Low TRI-STATE				mA
I_{CC}	Supply Current	V_{CC} = 5.5V 54/74ALS1243 A Port Outputs High A Port Outputs Low TRI-STATE				mA
I_{CC}	Supply Current	V_{CC} = 5.5V 54/74ALS1244 Outputs High Outputs Low TRI-STATE				mA

NOTE 1: See notes pg. 1-iii, figures pg. 3-2.

1

Switching Characteristics over recommended operating free air temperature range (Notes 1, 2)

Parameter (Propagation Delay Time)	Circuit Configuration	74ALS			54ALS			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Low-to-High Level Output								ns
T_{PHL}, High-to-Low Level Output	ALS 1240, 1242							ns
T_{PLH}, Low-to-High Level Output								ns
T_{PHL}, High-to-Low Level Output	ALS 1241, 1243, 1244							ns
T_{PZL}, Output Enable to Low Level								ns
T_{PZH}, Output Enable to High Level								ns
T_{PLZ}, Output Disable From Low Level								ns
T_{PHZ}, Output Disable From High Level	ALS 1240, 1242							ns
T_{PZL}, Output Enable to Low Level								ns
T_{PZH}, Output Enable to High Level								ns
T_{PLZ}, Output Disable From Low Level								ns
T_{PHZ}, Output Disable From High Level	ALS 1242							ns
T_{PZL}, Output Enable to Low Level								ns
T_{PZH}, Output Enable to High Level								ns
T_{PLZ}, Output Disable From Low Level								ns
T_{PHZ}, Output Disable From High Level	ALS 1241, 1243, 1244							ns
T_{PZL}, Output Enable to Low Level								ns
T_{PZH}, Output Enable to High Level								ns
T_{PLZ}, Output Disable From Low Level								ns
T_{PHZ}, Output Disable From High Level	ALS 1241, 1242							ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-2.

NOTE 2: Switching characteristic conditions are V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50pF.

Advanced Schottky

The DM54/74AS family of devices are designed to meet the needs of system designers who require the ultimate in speed. AS achieves the fastest prop delays bipolar technology can offer (2 ns per gate). The AS family also offers significant reduction in power dissipation (8 mw per gate) over present Schottky (54/74S) with toggle rate capability of up to 200 MHz.

The AS family is TTL pinout compatible and offers Schottky (54/74S) drive capability with better fan out, higher noise immunity and faster operation.

For maximum design flexibility and elimination of special drawings, the AS family will be introduced with $\pm$ 10% V_{CC} over the military and commercial full temp range as standard product. Furthermore, all switching characteristics are guaranteed over the full temperature and V_{CC} range.

National Semiconductor

ADVANCED SCHOTTKY

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC} (1)	7V
Input Voltage, V_I: All Inputs	7V
I/O Ports	5.5V
Off State (High Level) Voltage Applied to Open-Collector Outputs	7V
High Level Voltage Applied to 3-State Outputs	5.5V
Operating Free-Air Temperature Range:	
SN54AS	−55°C to 125°C
SN74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Recommended Operating Conditions

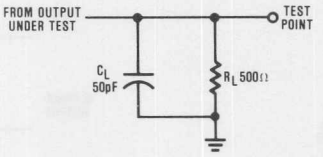
Parameter		Standard Output			Buffer Output			Bus Driver Output			Unit
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	54/74AS	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
High Level Input Voltage, V_{IH}	54/74AS	2.0			2.0			2.0			V
Low Level Input Voltage, V_{IL}	54/74AS			0.8			0.8			0.8	V
High Level Output Voltage, I_{OH} (2)	54AS			−2.0			−12			−40	mA
	74AS			−2.0			−15			−48	mA
High Level Output Current, V_{OH} (3)	54/74AS			5.5			5.5			5.5	V
Low Level Output Current, I_{OL}	54AS			20			32			40	mA
	74AS			20			48			48	mA
Operating Free-Air Temperature, T_A	54AS	−55		125	−55		125	−55		125	°C
	74AS	0		70	0		70	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

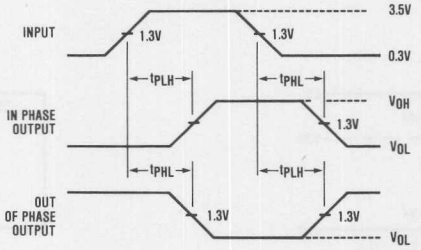
Parameter		Conditions		Standard Output			Buffer Output			Bus Driver Output			Unit
				Min	Typ(4)	Max	Min	Typ(4)	Max	Min	Typ(4)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2			−1.2			−1.2	V
V_{OH}	High Level Output Voltage (2)	I_{OH} = MAX V_{CC} = 4.5V					2.4	3.2		2			V
		I_{OH} = −2.0mA		V_{CC}−2V			V_{CC}−2V			V_{CC}−2V			V
I_{OH}	High Level Output Current (3)	V_{CC} = 4.5V V_{OH} = 5.5V				0.1			0.1			0.1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = MAX			0.35	0.5		0.35	0.5		0.35	0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V V_I = 7V				0.1			0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_I = 2.7V				20			20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.5V				−1.0			−1.0			−1.0	mA
I_O	Output Current (5)	V_{CC} = 5.5V V_O = 2.25V		−30		−110	−30		−110	−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied (6)	V_{CC} = 5.5V V_O = 2.7V							50			50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied (6)	V_{CC} = 5.5V V_O = 0.5V	I/O Ports						−1.0			−1.0	mA
			Non-I/O						−50			−50	μA
I_{CC}	Supply Current (7)	V_{CC} = 5.5V											mA

NOTE 1: Voltage values are with respect to network ground terminal.
NOTE 2: Does not apply to open-collector outputs.
NOTE 3: Applies only to open-collector outputs.
NOTE 4: All typical numbers are at V_{CC} = 5V, T_A = 25°C.
NOTE 5: The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.
NOTE 6: Applies only to TRI-STATE outputs.
NOTE 7: Refer to individual data sheet for I_{CC} limits.

Test Waveforms

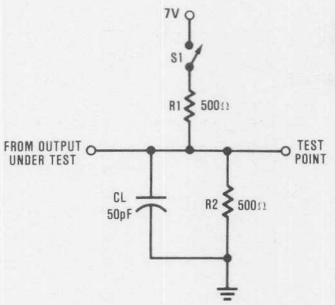


LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

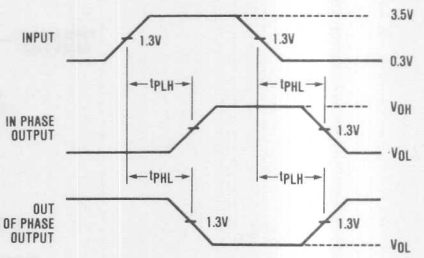


VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

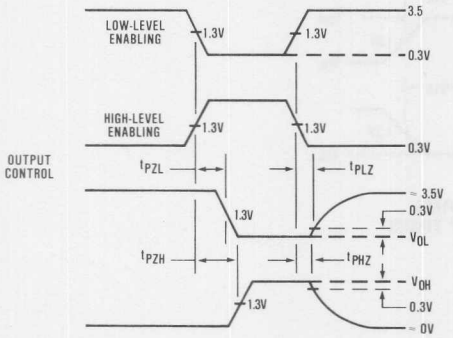
NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1MHz, Z_{OUT} = 50 Ω, $t_r = t_f$ = 2ns.



LOAD CIRCUIT FOR TRI-STATE OUTPUTS



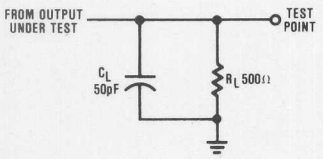
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



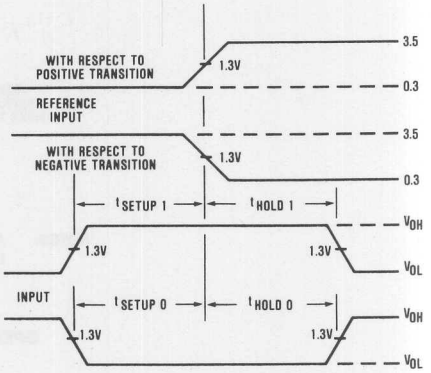
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, TRI-STATE OUTPUTS

Parameter	S1 Switch Position
T_{PLH}	OPEN
T_{PHL}	OPEN
T_{PHZ}	OPEN
T_{PZH}	OPEN
T_{PLZ}	CLOSED
T_{PZL}	CLOSED

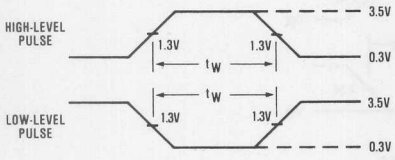
NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1MHz, Z_{OUT} = 50 Ω, $t_r = t_f$ = 2ns.



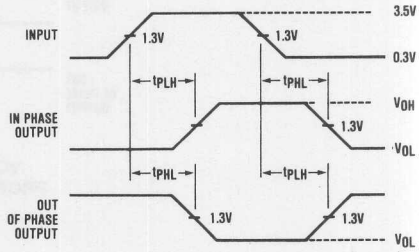
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



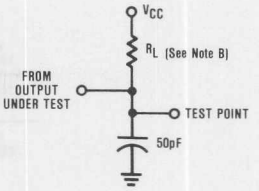
VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

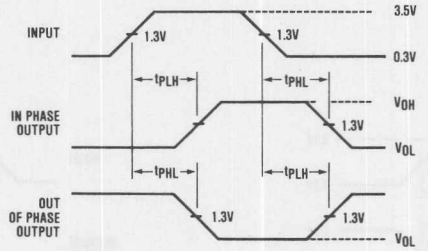
3

NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1MHz, Z_{OUT} = 50 Ω, $t_r = t_f$ = 2ns.



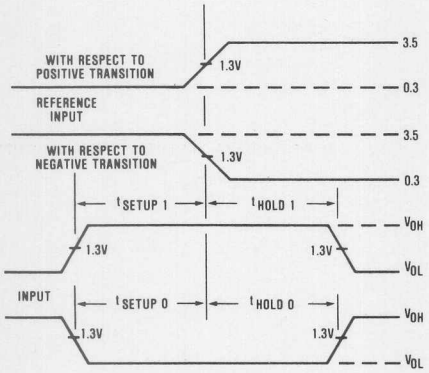
NOTES: A. C_L includes probe and jig capacitance
B. $R_L = 2K\Omega$ for standard outputs
$R_L = 667\Omega$ for buffered outputs

LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

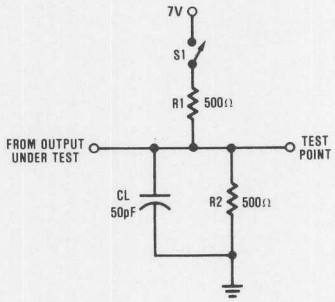


VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

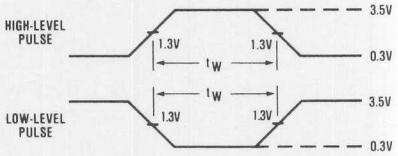
NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1MHz, $Z_{OUT} = 50\ \Omega$, $t_r = t_f = 2$ns.



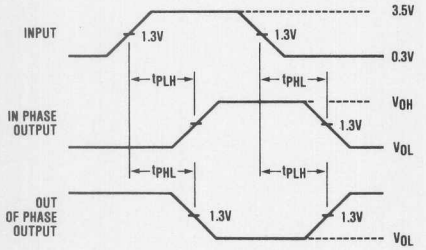
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



LOAD CIRCUIT FOR
TRI-STATE OUTPUTS

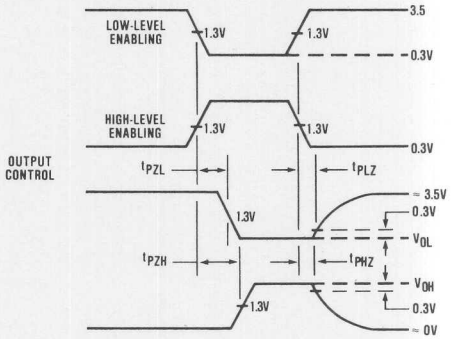


VOLTAGE WAVEFORMS
PULSE WIDTHS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

Parameter	S1 Switch Position
T_{PLH}	OPEN
T_{PHL}	OPEN
T_{PHZ}	OPEN
T_{PZH}	OPEN
T_{PLZ}	CLOSED
T_{PZL}	CLOSED



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, TRI-STATE OUTPUTS

NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1MHz, Z_{OUT} = 50 Ω, $t_r = t_f$ = 2ns.

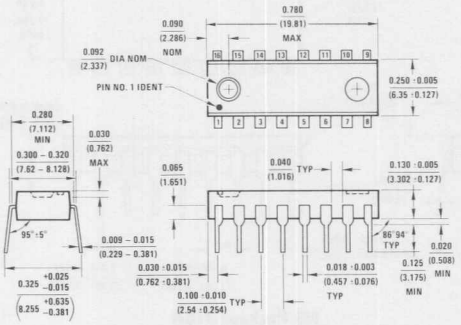
3

Appendices/Physical Dimensions

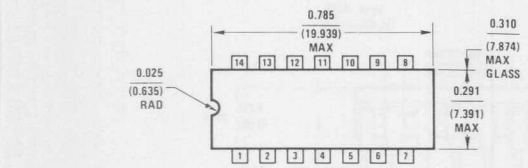
4

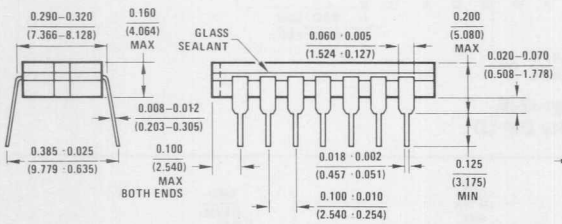
Physical Dimensions

All dimensions in inches (millimeters)

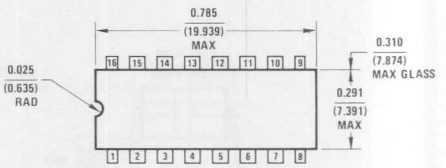


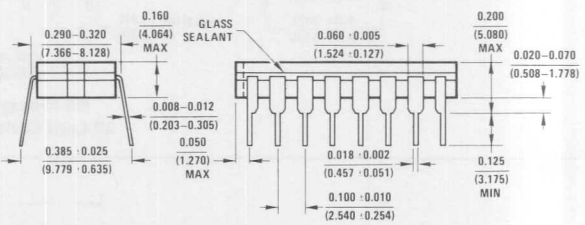
NS Package N16E
16-Lead Molded DIP (N)





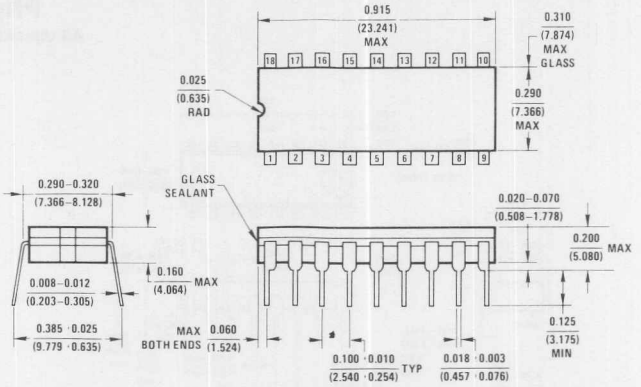
NS Package J14A
14-Lead Cavity DIP (J)



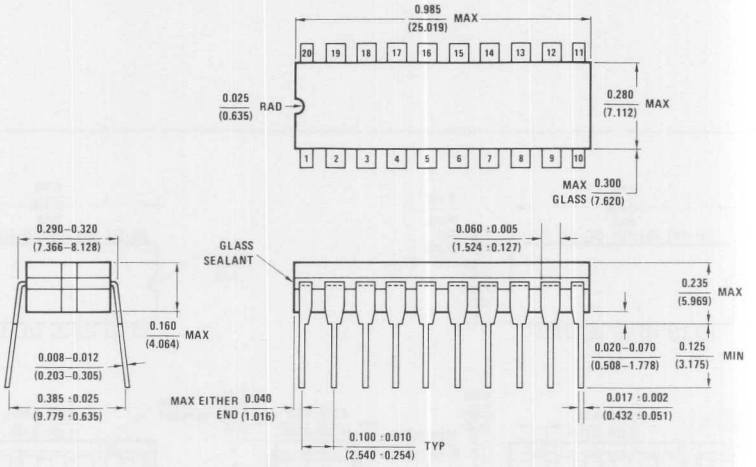


NS Package J16A
16-Lead Cavity DIP (J)

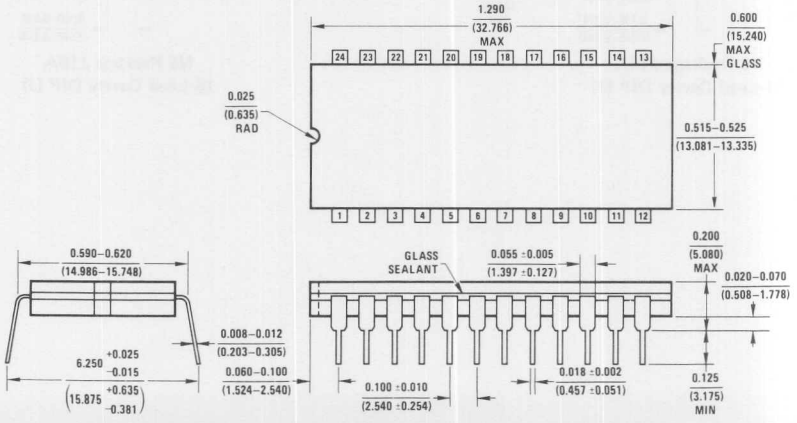
4



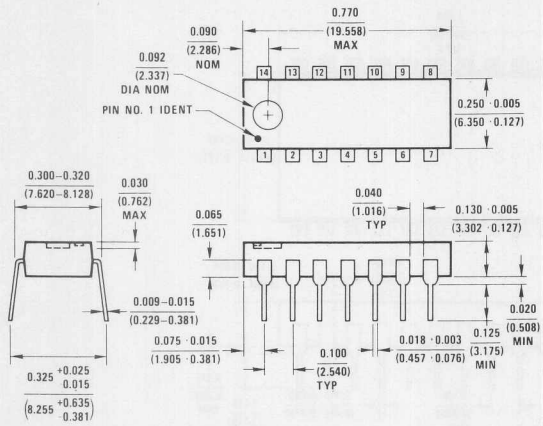
NS Package J18A
18-Lead Cavity DIP (J)



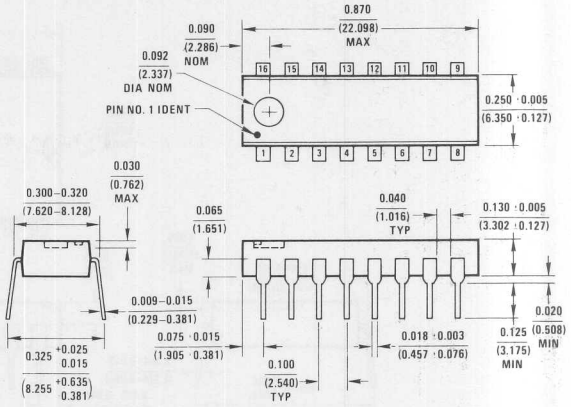
NS Package J20B
20-Lead Cavity DIP (J)



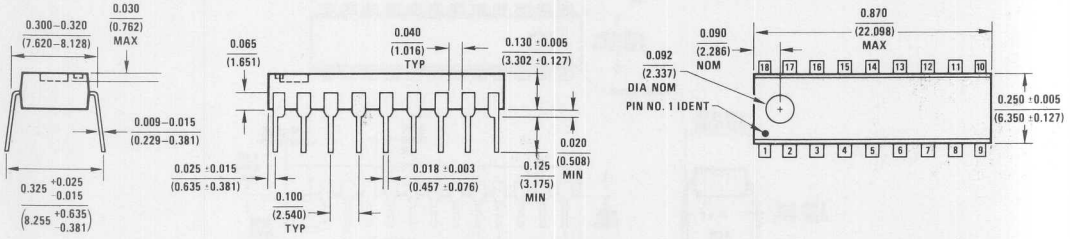
NS Package J24A
24-Lead Cavity DIP (J)



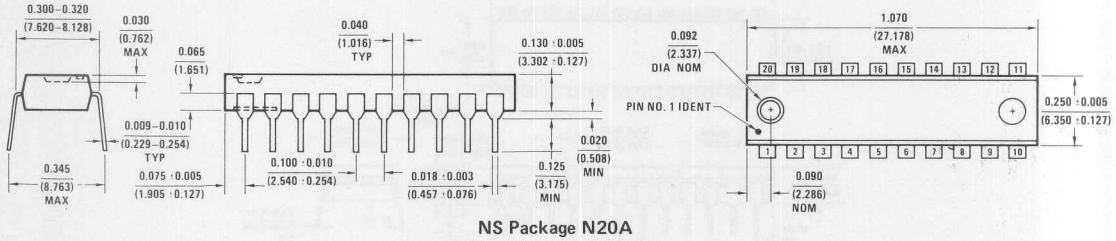
NS Package N14A
14-Lead Molded DIP (N)



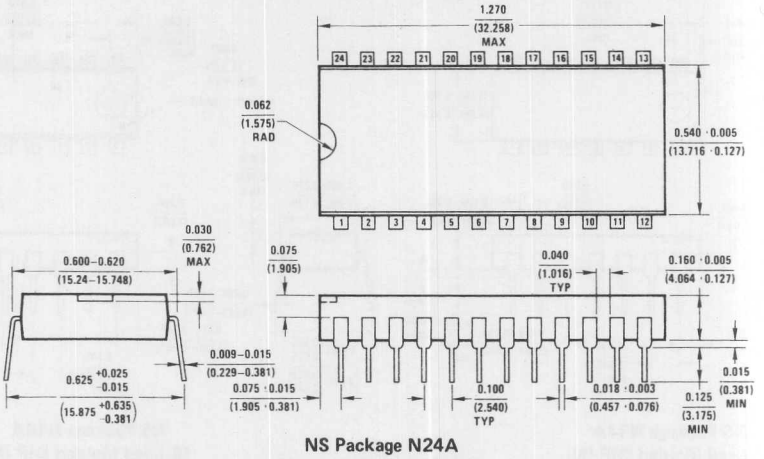
NS Package N16A
16-Lead Molded DIP (N)



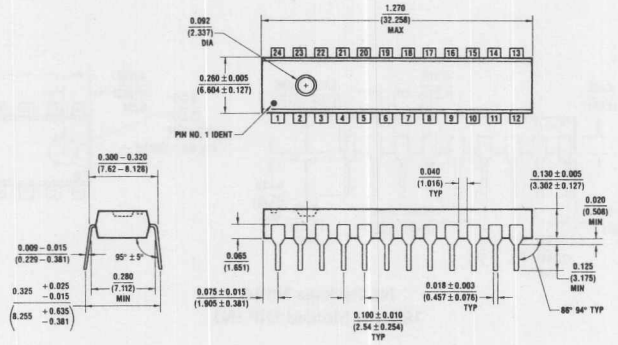
NS Package N18A
18-Lead Molded DIP (N)



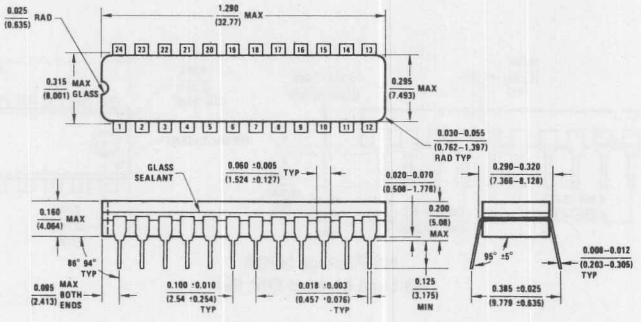
NS Package N20A
20-Lead Molded DIP (N)



NS Package N24A
24-Lead Molded DIP (N)



NS Package N24C
24-Lead Molded DIP (N)



NS Package J24F
24-Lead CERDIP (J)